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Assessment of Timing Requirements of Phasor Measurement Units

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<p>Accurate time synchronization of Phasor Measurement Unit (PMUs) play an important role in application of synchrophasor technology. Different time distribution methods are present which are capable of synchronizing Intelligent Electronic Devices (IEDs) with different timing accuracies. Initial part of this report presents information about some of the high-accuracy time distribution methods which were studied and evaluated based on their usability for synchrophasor applications. Later part of the report assesses timing requirements for PMUs by carrying out tests in a controlled experimental environment. In the past, generally PMUs were tested using a stand-alone relay test kit. A major drawback of this type of testing set-up is that it does not tests the PMUs in their practical operational environment which includes an instrumentation channel feeding input signals to the PMU. Overcoming this drawback, a new generic real-time Hardware-in-the-Loop (HIL) test set-up has been used to assess timing requirements of commercial PMUs in the laboratory. The results obtained showcase the effect of instrumentation channel on phase errors and also in determining timing requirements of PMUs. Insightful information showcasing the behaviour of PMU estimates in case of jitters in timing signals has also been presented.</p>		
Keywords: Phasor Measurement Unit, Time Synchronization, GPS, IIRIG-B, real-time HIL		

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Symbols and abbreviations

Abbreviations

<i>CT</i> :	Current Transformer
<i>CVT</i> :	Capacitive Voltage Transformer
<i>DFT</i> :	Discrete Fourier Transform
<i>FPGA</i> :	Field Programmable Gate Array
<i>GPS</i> :	Global Positioning System
<i>GUI</i> :	Graphical User Interface
<i>HIL</i> :	Hardware-in-the-Loop
<i>IC</i> :	Instrumentation Channel
<i>IED</i> :	Intelligent Electronic Device
<i>LAN</i> :	Local Area Network
<i>NTP</i> :	Network Time Protocol
<i>PDC</i> :	Phasor Data Concentrator
<i>PMU</i> :	Phasor Measurement Unit
<i>PPS</i> :	Pulse per Second
<i>PTP</i> :	Precision Time Protocol
<i>RMS</i> :	Root Mean Square
<i>ROCOF</i> :	Rate of Change of Frequency
<i>RTOS</i> :	Real-Time Operating System
<i>SOC</i> :	Second of Century
<i>UTC</i> :	Coordinated Universal Time
<i>VT</i> :	Voltage Transformer

1 Introduction

The modern power grid is a large complex and interconnected system. It continues to expand into even bigger and more interconnected system with transmission lines being pushed to their operating limits. The dynamics of the power system has become more challenging to model accurately and at the same time, real-time monitoring and control of the system has become a vital requirement to prevent outages. Any event occurring at one part of the grid may affect the operation of the whole system. Understanding these events requires a way to efficiently compare the rapidly changing state of the system at different locations of the grid at all instances of time [1]. For this purpose, PMUs are being used for synchronized phasor measurements helping with state monitoring, estimation and fault detection [2]. The synchronized phasor measurements by PMUs are called synchrophasors.

Accurate time synchronization of various PMUs spread over a wide network area with a common reference time is the key to effective real-time monitoring and control. To be able to monitor and control the interactions between different parts of the grid, first it is required to acquire and compare the state of the power system variables at different parts of the grid at the same time and at all time instants. This process highlights the importance of precise time synchronization of PMUs.

There can be major events like cascading faults leading to large blackout or inter-area oscillations which would require studies and analysis in hindsight to gain insight on the causes resulting to the disturbances and prevent them from reoccurring. PMUs installed at various locations of the grid generate big chunks of data which are being stored continuously [1]. To efficiently utilize the data from the files containing synchrophasor data from different locations and to be able to co-relate and comprehend the events happening at those locations requires establishment of a highly accurate common *Time Reference*. Hence it is required that PMU measurements are time stamped using a standard high accuracy reference time [3].

1.1 Aim

Time synchronization of PMUs and other substation devices helps achieving accurate system control and precise data acquisition. Correct operation standards of the PMUs have been defined in IEEE std. C37.242-2013 [3] and IEEE std. C37.118.1-2011 [4], and is dependent on a common and highly accurate timing reference. Over the period of time many time distribution solutions have come up for Intelligent Electronic Devices (IEDs). The first aim of this thesis was to study about and assess the performance of these synchronization solutions for their application in PMUs. The evaluation criteria is based upon the steady-state synchrophasor measurement requirements mentioned as in IEEE std. C37.118.1-2011 [4].

Another goal of this thesis was to investigate and evaluate the time synchronization requirements of PMUs by carrying out tests in a controlled experimental

environment. The time received by the PMU impacts the accuracy of PMU measurements and phasor estimation. Time received should be accurate enough to keep the PMU's performance within compliance limits as specified in the standard [4]. In the past, compliance of the PMUs have been tested using stand-alone relay test kits, for example in [6]. These test set-ups did not allow to test the PMUs in conditions similar to the practical on-field conditions. In the test set-ups like this, there is no *Instrumentation Channel* feeding signals to PMUs nor a method to vary the accuracy of PMU timing. So for this thesis work, the focus was to create a laboratory test set-up which facilitates in timing assessment of the PMUs without the constraints mentioned above.

1.2 Thesis outline

The thesis report is organized in following chapters:

Second Chapter presents the basic ideas and concepts used throughout the thesis.

Third Chapter presents various timing sources for IEDs and evaluates them based on their usability for commercial PMUs.

Fourth Chapter discusses the importance of accurate timing for PMU for correct operation and details some previous work done in this area.

Fifth Chapter presents the new approach and discusses the real-time, HIL test set-up to examine the time source requirements of a commercial PMU in practical applications.

Sixth Chapter presents results of the tests conducted.

Seventh Chapter presents summary, conclusion and future work.

2 Synchrophasor Technology and Relevance of Timing

2.1 Introduction

Periodic sinusoidal signals, for a constant frequency are commonly represented as phasors for analysis purposes. In time domain, a periodic sinusoidal signal shown in Fig. 2.1 could be mathematically represented by

$$x(t) = X_m \cos(\omega t + \phi) \quad (2.1)$$

Here ω is the angular frequency of the signal, ϕ is its phase angle with respect to a fixed reference frame and X_m is the peak of the signal. Phasor representation of the signal in eq 2.1, defined for angular frequency ω is as shown in eq. 2.2 to 2.4:

$$X = \frac{X_m}{\sqrt{2}} e^{j\phi} \quad (2.2)$$

$$= \frac{X_m}{\sqrt{2}} (\cos(\phi) + j\sin(\phi)) \quad (2.3)$$

$$= X_r + jX_i \quad (2.4)$$

Where the magnitude of the phasor is given by the root-mean-square (rms) value of the waveform and subscripts r and i denote the real and imaginary parts of the complex value in rectangular components [4].

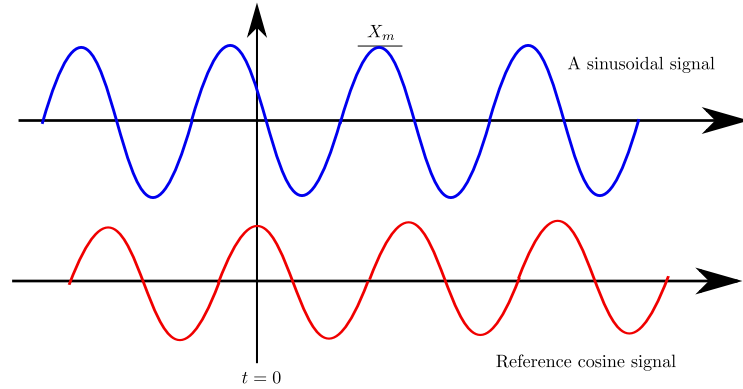


Figure 2.1: A periodic sinusoidal signal to be sampled and measured by a PMU and a reference cosine function synchronized to UTC for time reference.

2.2 Synchrophasors

According to IEEE Standard C37.118.1-2011, a synchrophasor is a phasor representation of a signal where the phase angle (ϕ) is the instantaneous phase angle

difference between the measured signal and a reference cosine function at nominal system frequency synchronized to Coordinated Universal Time (UTC) [4]. For the sinusoidal signal X and reference cosine function shown in Fig. 2.1, synchrophasor would be given by eq. 2.2 and ϕ would be the instantaneous phase angle difference. With a fixed temporal reference, synchrophasor measurements could be used to determine useful information about important operational parameters of the grid.

According to the above definition, for the signal $x(t)$ shown in Fig. 2.2 and expressed by equation 2.1, in a 50Hz system, its synchrophasor angle would be 0° if $x(t)$ has a maximum at the UTC second roll-over. The synchrophasor angle would be -90° in case when the signal $x(t)$ would be at zero and moving towards positive at the UTC second roll-over. Synchrophasor phase angles are generally represented with angles between -180° and 180° . [4]. Three phase quantities can be represented using three individual phasors with magnitude and phase angle. For a balanced three phase system, the phasors of a three phase quantity would have same magnitude but different phase angles which would be equidistant and stationary with respect to each other.

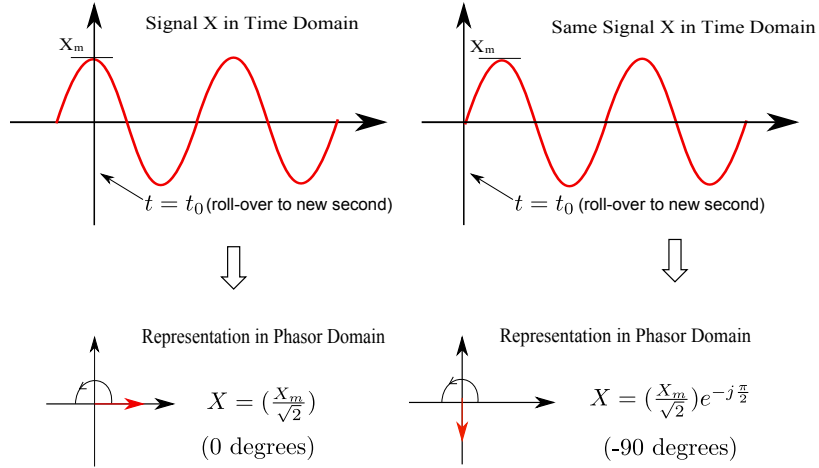


Figure 2.2: Convention for synchrophasor representation

2.3 Synchrophasor Measurement System

A basic synchrophasor measurement network is made up of hierarchical layers of PMUs and PDCs connected by a robust communication network [5]. Apart from the communication technologies, the other two components are discussed below in brief:

- **PMUs:** These devices sample signals, estimate time-stamped phasors, frequency and rate of change of frequency (ROCOF) and transmit the estimated

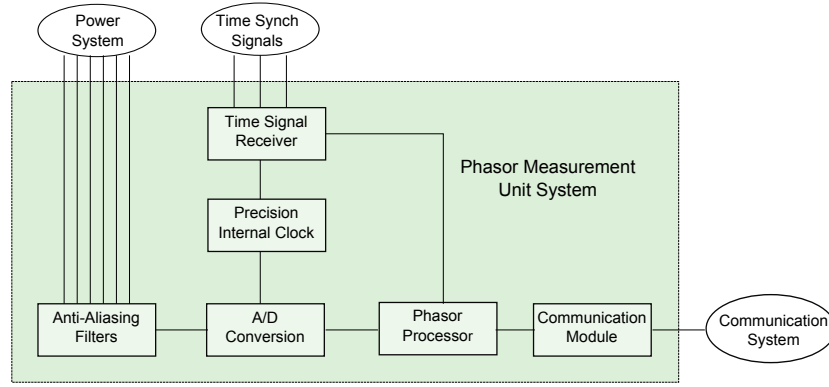


Figure 2.3: A general PMU structure consisting various functional components

phasors to Phasor Data Concentrators (PDCs). Fig. 2.3 shows the basic structure and functional components of a PMU device. PMUs transmit synchrophasor data packets standardized by a protocol given by IEEE C.37.118.2. [5]. There are four types of synchrophasor message frames described in the standard:

- *Data*: These contain measurements made by PMU.
- *Configuration*: Machine readable message describing the data types, calibration factors, and other meta data for the data that PMU/PDC sends.
- *Header*: Human readable descriptive message provided by the user.
- *Command*: Machine readable codes sent by PMUs/PDCs for control and configuration.

All synchrophasor measurements shall be tagged with the UTC time corresponding to the time of measurement. The message frames include the time stamps in from of an 8-byte message consisting three parts: a 4 byte Second of Century (SOC), a 3 byte Fraction of Second (FRACSEC) and a 1 byte Time Quality indicator [5]. SOC is the count of seconds from UTC midnight (00:00:00) of January 1, 1970 till the current second. Leap seconds are also added to or deleted from the count to keep it synchronized with the UTC. FRACSEC count represents the fraction of current second as an integer and is zero at the second roll-over [5]. Detailed information on synchrophasor message frames and time tags can be found in [5].

- **PDCs**: These devices are computers capable of receiving phasor data streams from multiple PMUs and even other PDCs. Main function of PDC is time alignment of phasor data received from multiple sources to create a phasor database which could be stored or sent to computers in operation centers for further applications of PMU data from different sources [5]. PDCs can also be useful in monitoring PMUs performance.

Each substation can have multiple PMUs connected to a PDC computer. This PDC computer collects the measurements and forward the data to mid-level, regional

PDCs. There can be several layers of PDCs serving applications like monitoring, data-storage and control [5]. A simple structure of PMU and PDC network for synchrophasor technology application is shown in Fig. 2.4.

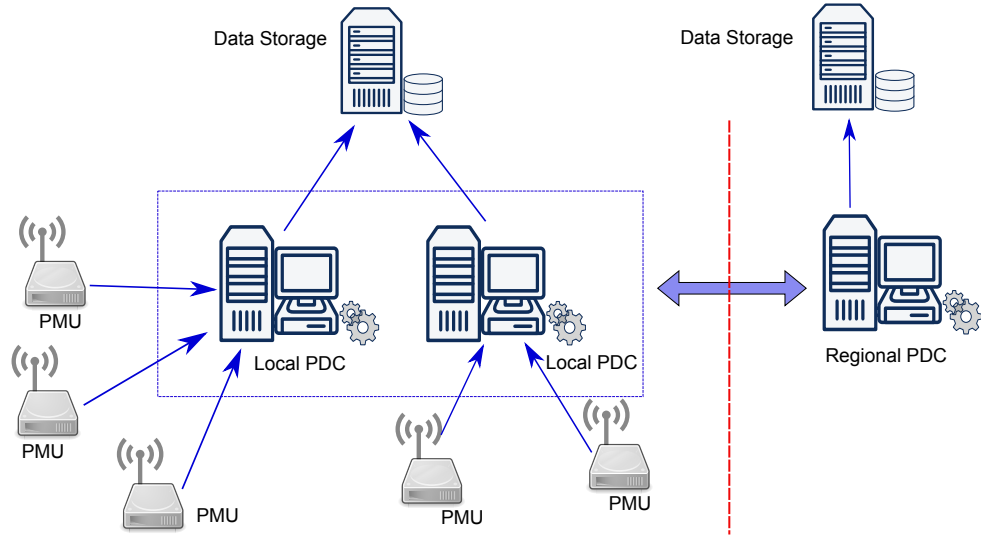


Figure 2.4: A typical synchrophasor network

2.4 Importance of time synchronization

PMUs continuously sample and measure the instantaneous voltage, current and frequency at various locations over a wide area of the power grid. The measured phasor values are then reported to PDCs for further analysis and archives. If all the PMUs sample various signals synchronously using a common time reference, then their phasors which are reported from different locations across the network can be put on a single phasor diagram. This enables the grid operators to effectively monitor the states of the system at various location in real-time. For a big network, such wide scale real-time monitoring leads to high resolution situation awareness of the grid.

To facilitate such high resolution awareness, all the quantities measured by PMUs are time-stamped and synchronized to the UTC time using a high accuracy time source. These time-stamps can be used to aid in comparing data from different sources when reconstructing the lead-up to a power system event or when merging data from multiple sources into one data stream (done by PDCs). Fig. 2.5 shows the essence of synchronized sampling and time-stamping by PMUs over a wide area network.

One important thing to note is that to maintain the significance of accurate time-stamps, PMUs compensate for all the delays caused in signal measurement and filtering while time stamping the samples. This procedure is known as source based

group delay compensation and allows various time-stamped phasors from different PMUs to be aligned in a single temporal frame regardless of type of filtering process or reporting rates used by different PMUs [7].

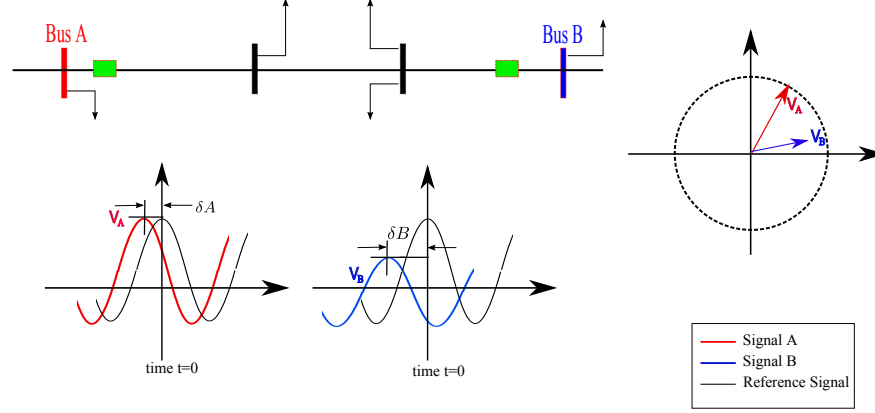


Figure 2.5: Synchronized sampling and phasor representation using same temporal frame

If PMUs or a single PMU shifts away from accurate UTC synchronization, it can lead to unintentional obscurity of the state of the grid where the algorithms using PMU data would receive erroneous representation of the grid. Event reconstruction or merging PMU data could give unfathomable results. Fig. 2.6 shows the effect of time skewing on the phasor estimation by the PMUs. This could be catastrophic for any control or protection function utilizing the corrupted phasors from such a PMU. Through out this report PMU time synchronization error has also been interchangeably mentioned as a ‘time skew’ problem.

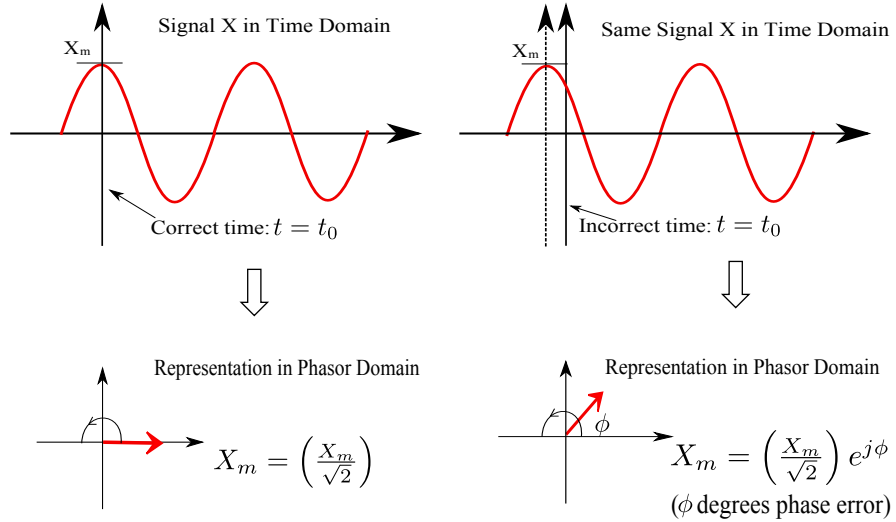


Figure 2.6: Effect of time skew on Phasor estimates by PMUs

2.5 Types of time synchronization errors

Synchronization of synchrophasor is achieved using two time keeping components: External timing signal and PMU's internal sampling clock. So, fundamentally there could be two types of time skew causes in PMUs:

- Internal Synchronization Errors:** This type of time skew errors are caused due to unintentional drifting of internal clock of PMUs away from the accurate UTC time. Most of the practical PMUs receive one Pulse per Second (PPS) timing signals from GPS clocks and the PMU internal sampling clock is then synchronized to this signal every second [9]. Now, these clocks running inside PMUs are responsible for time-stamping the measured samples. However, the sampling clocks of PMUs might not be exactly synchronized between the two consecutive PPS pulses due to inaccuracy of internal clocks and time skew problems could originate between measurements from different PMUs. In these types of synchronization errors the PMUs may or may not be able to attain synchronization after drifting. Figures 2.7 and 2.8 display two real life examples from the field showing drifting of PMU's internal clock. The voltage measurements for a PMU shown as example in Fig. 2.7 has lost its internal clock synchronization and is not able to regain it even after receiving PPS signals from GPS.

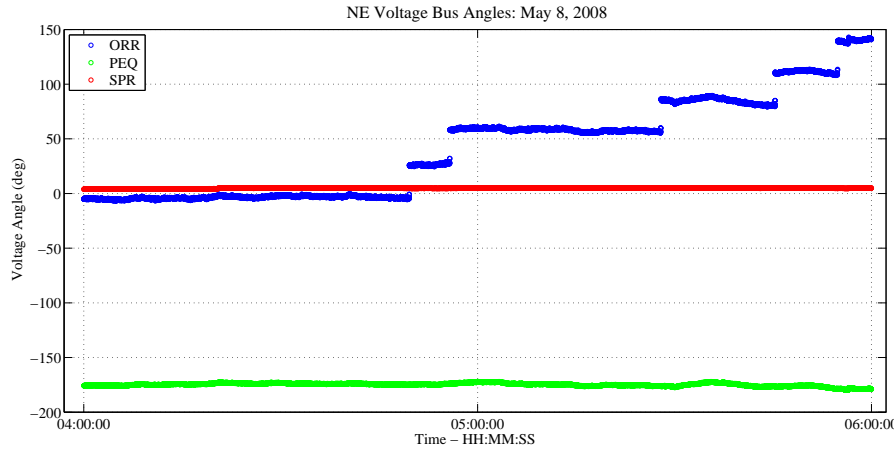


Figure 2.7: Error in voltage angle measurement caused due to internal clock's time skewing in PMU at ORR, The PMU is not able to regain synchronization in this case. This figure is courtesy Commission Federal de Electricidad Mexico.

- External Synchronization Errors:** External time skew problems could arise due to causes like unavailability of timing signal or corruption in timing signal. The time provided by a timing signal could also be erroneous making the particular PMU or a group of PMUs lag or lead the actual UTC timing. Fig. 2.9 shows a real life example of a PMU losing its GPS signal.

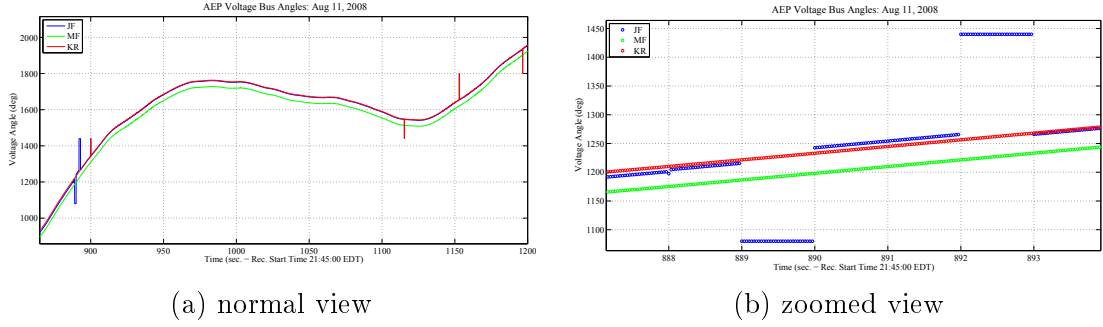


Figure 2.8: Error in voltage angle measurement caused due to internal clock's time skewing in PMU at ORR, This PMU regains synchronization after every one second pulse form GPS. This figure is courtesy Commission Federal de Electricidad Mexico.

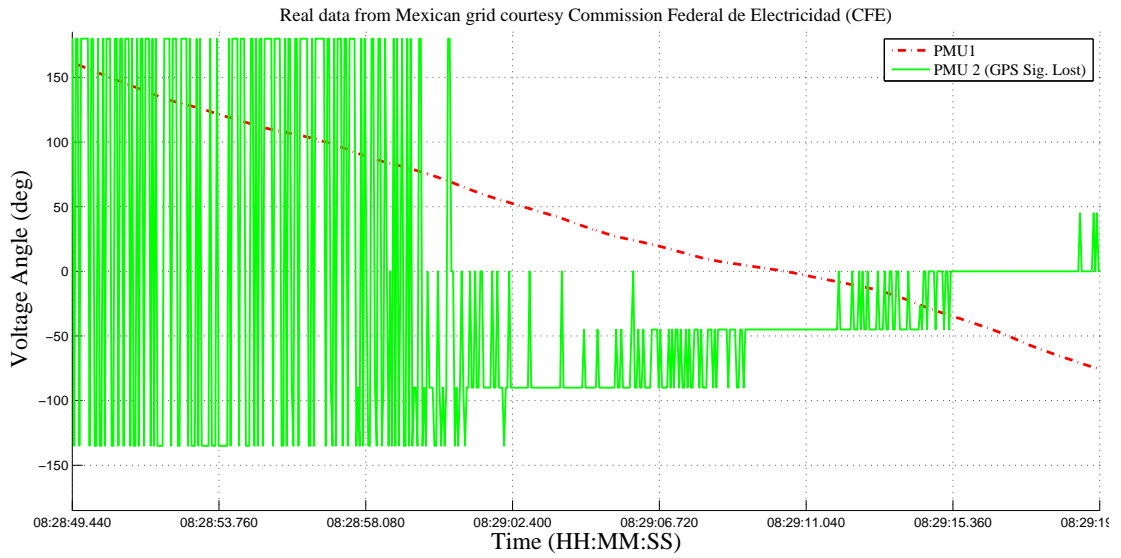


Figure 2.9: Error in voltage angle measurement in PMU 2 caused due to loss of the GPS timing signal. This figure is courtesy Commission Federal de Electricidad Mexico.

There are various other examples available showing different time skew problems, for example as documented in [8] and [9].

In this chapter, importance of correct timing and synchronization PMUs were shown for efficient utilization of synchrophasor technology into many monitoring and control applications. Examples of different types of time-synch errors in PMUs were also shown.

3 Timing Solutions for PMUs

3.1 Introduction

One of the objective for this thesis was to assess the available timing solutions which are being utilized already or could be utilized in near future as a time source of PMUs. This chapter provides an insight into different types of timing options available and analysis of those sources in view of usability for synchrophasor application.

3.2 Time Distribution Methods

Need for time synchronization has been there since modernization of substation monitoring and protection devices and need for communicating time framed information has become important. Over time, many timing sources and time distribution methods from the sources to Intelligent Electronic Devices (IEDs) have emerged. Different methods are capable in providing time with varying accuracies and are employed in various processes depending upon the requirement by the devices. The most common of the present time sources is GPS and the most common time distribution method is Network Time Protocol (NTP)[10].

Other major time sources are the radio clock receivers that receive standard radio transmission of time from ground based radio stations like WWVB (US) and DCF77 (Germany). Other time distribution methods include Pulse Per Second (PPS), IRIG-B coded time signals and IEEE 1588 Precision Time Protocol (PTP) [7]. A brief overview of these sources and distribution methods is presented below:

- **GPS Time Source:** GPS is a system of satellites made up of a constellation of 24 active satellites orbiting the earth. All of these satellites also have on-board atomic clocks that keep highly accurate time which is in the range of ± 0.3 ns. These satellites transmit GPS signals containing high-accuracy time information from the on-board atomic clock. These signals can be received by GPS receivers anywhere across the world with a very high accuracy within ± 200 ns of UTC [10]. All these factors make GPS timing signals a very suitable option for PMU timing.

There are a few drawbacks associated with GPS timing solution. Apart from maintaining connections from four different satellites at all times, a few other factors could also affect the performance of GPS based timing solutions. Open unobstructed view of sky for the receiver antenna is a must. Factors like atmospheric delays, signal multipath interference and satellite orbital errors can also affect its performance and are out of human control [10]. But still, taking all these factors into account, the over all performance and accuracy of the GPS makes it a well suited time distribution methods for synchrophasor applications.

- **Standard Radio Transmission:** In standard radio distribution of time the receiver device periodically synchronizes its clock to the real atomic clock whose time is transmitted using radio waves. Radio station's atomic clock is highly accurate with respect to the UTC but the unaccounted propagation delay for the radio signals significantly affects the over-all accuracy of this timing method. The propagation delays can cause a delay upto 30 ms.

Distribution of time from a chosen time source like GPS or radio receiver to various IEDs can be done using different methods. Some of the most used methods are listed below:

- **Network Time Protocol (NTP):** This is the most widely used time distribution protocol in the world and almost every computer connected to internet uses this protocol for time synchronization [7]. NTP uses a network of devices and computers acting as time servers, clients and interconnecting transmission path at different hierarchical levels called stratum. Each device at one stratum serves as a time server to devices at lower stratum. Primary servers at *stratum one* are connected to a high accuracy atomic clock or a receiver based time source [10]. The basic principle of implementation is that each client (lower level device) sends periodic requests to the upper level time servers for current time stamps. After receiving time stamps from different time servers, the internal algorithm at the client selects the best time server and synchronizes its time with the chose time server.

In most NTP implementations, stratum one is located in internet, stratum 2 near the gateway and stratum 3 and 4 at the Local Area Network (LAN)[11]. NTP is built on the Internet Protocol (IP) and uses User Datagram Protocol (UDP) and its implementation is pure software which means that the time-stamps are taken at the application layer [11]. One advantage of using NTP for time distribution method is that it is distributed using already existing Ethernet cables so no extra infrastructure is required for the implementation. The accuracy of NTP is in the range of 10 to 250 ms and depends on the factors mentioned below [11], [10]:

- network topology and congestion leading to asymmetry in propagation delays between client and server.
 - Operating system delays caused by fluctuations in network protocol stack between application layer and physical layer.
 - The medium of communication between clients and servers
 - Time stamp measurement errors and
 - Accuracy of the primary clock.
- **PPS:** It is a high-accuracy time pulse originating from precision clocks like a GPS receiver that very precisely indicates the start of a second [1]. With

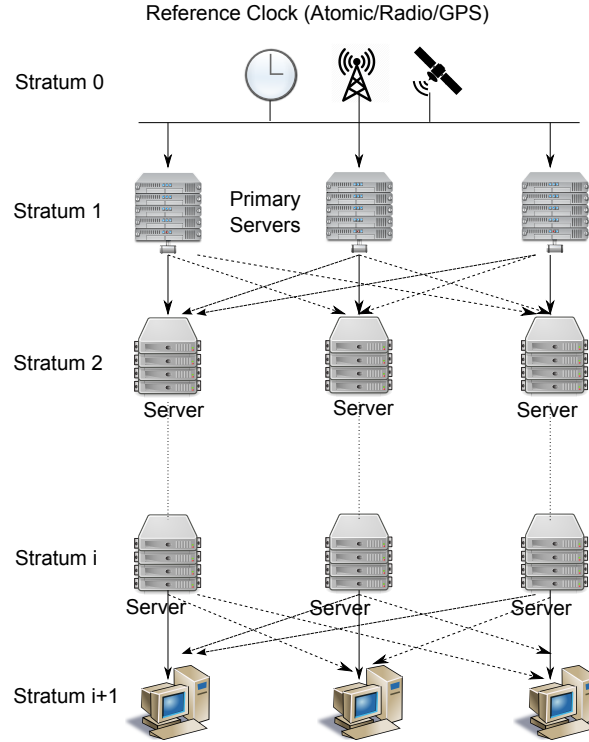


Figure 3.1: A typical NTP hierarchy [11].

distribution of one pulse per second, the internal clock of the PMU or any other IED can be synchronized with the rising edge of the pulse as a marker for second roll-over. However the pulse cannot be associated with any particular time instance. To resolve this ambiguity another data channel is required [1].

- **IEEE 1588:** It is a standard protocol for precise time synchronization in packet based networks that support multicasting [11]. Time distribution through PTP protocol is capable of achieving accuracy as high as ± 100 ns [7]. However, this is only possible by using dedicated hardware for precise time-stamping of the Ethernet frame's arrival and departure time. This is known as hardware-assisted software implementation of PTP and is shown in a very basic form in Fig. 3.2. Hardware assisted methods generate and create timestamps as close as possible to the physical layer which leads to a very high accuracy [11]. Software only implementation of PTP, shown in Fig. 3.2 also exists in the industry where the whole protocol is implemented in software level including the time-stamping of the packets. This however results in reduction of accuracy as compared to hardware-assisted implementation of the protocol. For software only implementation, depending upon the operating system, errors in the range of hundreds of microseconds to milliseconds are introduced into the timestamps [11].

IEEE 1588 is important for electric utilities because of its high accuracy while reducing the cost to install and maintain a separate dedicated timing network.

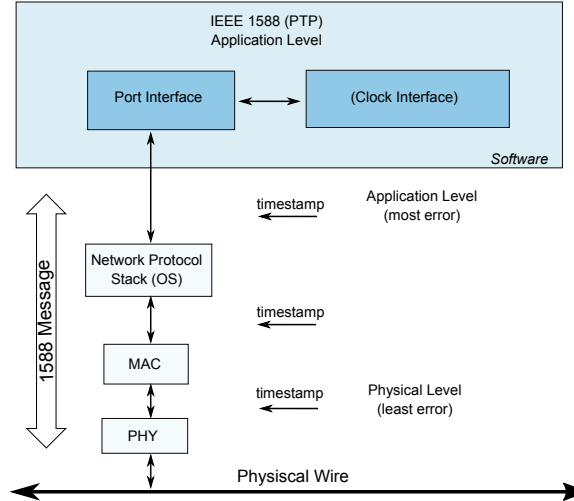


Figure 3.2: IEEE-1588 hardware and software only implementations [11].

With 1588, the cabling infrastructure requirement is reduced by allowing time synchronization information to be transported over the same Ethernet medium as the data communications. Time signal using IEEE 1588 PTP can be carried out for long distance throughout the network and converted to IRIG-B for synchronization of existing devices that are not capable of 1588, allowing them to be kept in service even while updating the timing and data network infrastructure [12]. While on the other hand, implementation of hardware assisted PTP based time distribution requires for all the network devices (all Ethernet switches) to have the hardware support for high-precision time stamping. For existing LANs, this is not feasible as this will require replacement of older network components with components that provide hardware assistance for time-stamping. At this time, the hardware support in relays and other substation IEDs remains limited [7].

- **IRIG-B:** This is one of many standardized sets of time-code formats documented in the IRIG Standard 200-4 [27]. Out of various standards, IRIG-B has become a popular format for time distribution to IEDs [7]. IRIG-B provides time once a second containing information from *second of the minute* to the *day of the year* in a binary coded decimal (BCD) format. IRIG-B standard also allows many different configuration designated as IRIG-B xyz , where, x , y z denote modulation technique, bit count and bit interval respectively. The most commonly used forms are unmodulated versions of IRIG-B [7]. With GPS as source, unmodulated IRIG-B can distribute time with an accuracy of ± 500 ns [7].

IRIG-B is used from short to medium distance applications such that there wont be any requirement for propagation delay compensation at the receivers [7]. IRIG-B is usually distributed using coaxial cables or fiber-optic cables

giving it excellent shielding quality of the signal [7]. On the other hand, this coaxial cable is an additional infrastructure and a single output can only drive a limited number of devices, depending on cable length and device load. These restrictions limit the scalability and increase deployment and maintenance costs for IRIG-B [12].

3.3 PMU Time Synchronization

Correct operation of PMUs for synchrophasor applications requires a common and accurate timing reference for sampling and time-stamping processes [3]. This timing reference as described in Section 2.2, establishes a relation between the UTC and the signal to be measured. To achieve this required time synchronization with UTC, the PMU need to be provided with timing signals. The source of accurate timing signals could either be internal (embedded in PMU) or supplied to PMU via suitable time distribution methods.

The time synchronizing signal fed to the PMU should be accurate enough to keep PMU's performance parameter *Total Vector Error (TVE)* within statutory limits. TVE is an expression of difference between the theoretical/actual phasor value of the signal and the phasor estimate of the signal given by the PMU under test at the same instant in time [4]. The estimated value of the phasor generated by a PMU can differ in both amplitude and phase from the actual/theoretical value of the phasor. The difference between these values is normalized and expressed as per unit of the theoretical value as defined in equation 3.5.

$$TVE(n) = \sqrt{\frac{(\hat{X}_r(n) - X_r(n))^2 + (\hat{X}_i(n) - X_i(n))^2}{(X_r(n)^2 + (X_i(n)^2)}} \quad (3.5)$$

Where, $\hat{X}_r(n)$ and $\hat{X}_i(n)$ are the real and imaginary parts of the estimated phasor from sample index n and $X_r(n)$ and $X_i(n)$ are the real and imaginary parts of the actual phasor for index n .

The limit for TVE for synchrophasor measurements in steady-state conditions has been set at $\pm 1\%$ [4]. The quality of synchrophasor measurements is evaluated by calculating the TVE based on PMU estimates using equation 3.5. The TVE would be high if the PMU estimates are incorrect due to incorrect timing. So, the PMU timing signal should be accurate enough to so that PMU maintains its synchronization with the UTC and its TVE should not exceed the $\pm 1\%$ limit. Apart from the accuracy requirement, the timing source should also be available, without interruption at all the measurement location across the PMU network. So a timing signal suitable for synchrophasor applications should be suitable in terms of accuracy, reliability and availability [3].

For PMUs installed in a network with system frequency of 50 Hz, a time error of $1 \mu s$ corresponds to a synchrophasor phase error of 0.018° . Even with no magnitude

error in a phasor estimate by a PMU, just the phase error of 0.573° or 0.01 radians will cause 1% TVE as defined by equation 3.5. For a 50 Hz system, this phase error correspond to an error of $\pm 31.8 \mu\text{s}$. Similarly for a 60 Hz system, a timing error of $\pm 26 \mu\text{s}$ will result in 1% TVE in the phasor estimates. This thesis work was done at SmarTS Lab at KTH in Sweden, where, system frequency is 50 Hz. Hence from here onwards the default system frequency is taken to 50 Hz unless it is mentioned otherwise.

So, for a PMU to comply with the 1% TVE rule, the bare minimum requirement for any timing source in terms of its accuracy is that its accuracy should be better than $\pm 31.8 \mu\text{s}$.

In view of the the accuracy of the timing sources discussed in Section 3.2, time distribution methods which are suitable for synchrophasor applications are:

- GPS and PPS: dedicated GPS receiver for a PMU feeding the GPS signals directly to the PMU or a GPS based clock feeding multiple PPS signals to a group of PMUs.
- GPS and IRIG-B: combination of GPS based clock as primary time source feeding timing signals to multiples devices using IRIG-B.
- IEEE 1588 PTP: Hardware assisted implementation of the protocol.

Although from availability point of view, hardware support for PTP in the substation IEDs and Ethernet switches in the network remains a bottleneck in the implementation of PTP based timing distribution in substations. Use of IRIG-B is a good option for substation or control center level where time from a primary device could be distributed to a group of PMUs over a short distance using coaxial cables. Stand-alone PMU device, would require a GPS receiver to maintain synchronization.

So, at current stage, most feasible option for PMU time synchronization are either dedicated GPS receivers for separate PMUs or a combination of GPS receiver with the distribution methods like PPS/IRIG-B to distribute time to a group of PMUs in substations and control centers.

4 Time synchronization and Effect of Instrumentation Channel

In the previous section, we discussed PMU time synchronization methods and found out that, with available technology, a combination of GPS as a source and PPS or IRIG-B as time distribution methods is best suited for synchrophasor applications both in terms of accuracy and availability. Other technologies like IEEE 1588 PTP could be a time synchronization solution in near future. The performance of these methods should be evaluated based on the TVE compliance criteria of the PMUs.

As mentioned in Section 3.3, the accuracy of a phasor estimate by a PMU is measured in terms of TVE. In steady-state conditions, to be compliant with the standard, TVE of synchrophasor estimates by a PMU should be less than $\pm 1\%$. TVE is composed of errors in both phase and magnitude estimates. Accuracy of the PMU time synchronization, will directly affect the phase errors of the PMU. Phase error in PMU estimates is composed of various components like time source error, phase error or group delay in PMUs signal sampling and processing unit which includes analog to digital converters and step down transformers. The phase error caused by the inaccuracy or unreliability of PMU timing source would add up with other sources of error to increase the TVE. The compliance criteria for a TVE $< 1\%$ would become a limiting factor for phase errors caused by timing inaccuracies.

Apart from the factors mentioned above which contribute for phase errors in phasor estimates, there is one more external cause. In substations, a group of devices referred to as the Instrumentation Channel (IC) feeds scaled replicas of high amplitude current and voltage signals to the PMUs. In practical conditions this instrumentation channel also degrades the original signal in terms of phase and magnitude.

The first set of components in the instrumentation channel are instrument transformers: current and voltage transformers (CTs and VTs). Capacitive Voltage Transformers (CVTs) are used in high voltage substations. These devices do the transformation of power system voltages and currents to appropriate levels for feeding devices like relays, fault-recorders and PMUs.

Control cables form the other part of the instrumentation channel which constitute the secondary circuit wiring of the instrument transformers and then transport signals to the substation relays or PMUs. This wiring, generally, is not instrumentation class wiring and instead is control type wiring (non-twisted pairs)[14]. A typical instrumentation channel feeding current and voltage signals is shown in Fig. 4.1.

Output 2° of these instrument transformers have both magnitude and phase angle error. These CTs and VTs feed already phase shifted signals to PMUs. Phase angle errors in CVTs are randomly distributed in the range of $[-2^\circ, 2^\circ]$, whereas, phase

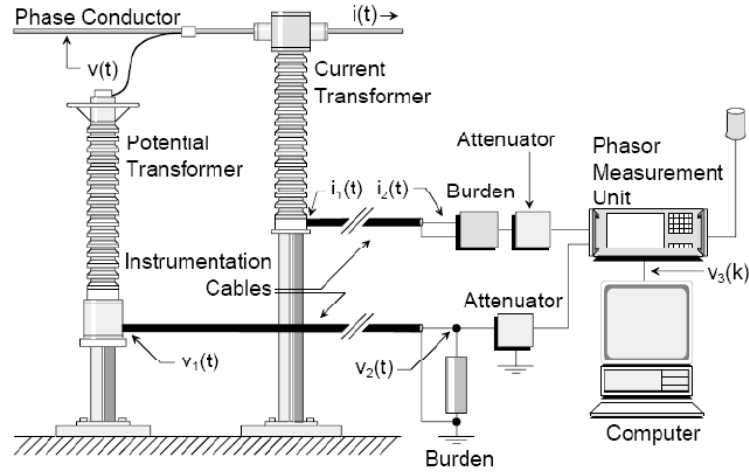


Figure 4.1: Typical current and voltage transformers instrumentation channel. [14]

errors in high accuracy VTs is in the range of $[-0.1^\circ, 0.1^\circ]$. Similarly, phase errors in high accuracy CTs are also in the range of $[-0.1^\circ, 0.1^\circ]$ [15]. These errors could increase significantly during the transients especially for CVTs as characteristic parameters of the constituting components deteriorate for frequencies other than the fundamental [14]. The use of isolating switches, grounds on the secondary circuits, and presence of non-linear burden are other factors which can have a significant impact on the accuracy of the over all instrumentation channel [14].

From phasor diagram analysis of simplified CT and VT representation, it can be observed that, the phasor of the output voltage signal of a VT lags the phasor of VT input signal. Due to this phase error, the output of the VT lags its input by a quantifiable amount of time. Similarly, the CT output current leads the original CT input current waveform in time. This is due to non-linearity of the constituting materials of the transformers. These misalignment in time between input and output signals is called the error in phase. For notational purpose, it was assumed that the

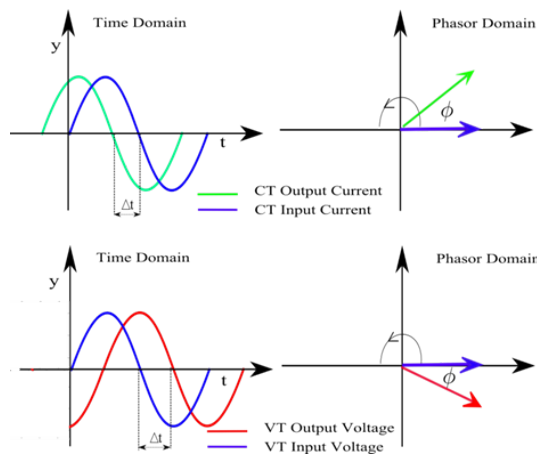


Figure 4.2: Phsors representation of CT and VT outputs

lagging phase error in the VTs is *positive* phase error and the leading phase error in the CTs is *negative*. A basic representation of the leading and lagging phase errors is shown in Fig. 4.2

In paper [16], the author presents a new term called *Global TVE*. This term includes two parts: the TVE caused by PMU itself which is labelled TVE_{PMU} and the errors caused of inaccuracies due to instrumentation channel (instrument transformers and control cables) which labelled as TVE_{IT} . Application of the Global TVE is illustrated in Fig. 4.3. In this Figure, U is the phasor representing the IC input signal at the high voltage side, Y represents the signal being fed to the PMU after being processed by the IC and \hat{Y} is the phasor estimate given by the PMU. The TVE Global relates \hat{Y} and U , and this concept can be helpful to assess the timing requirements of PMUs considering the contribution of all IC elements.

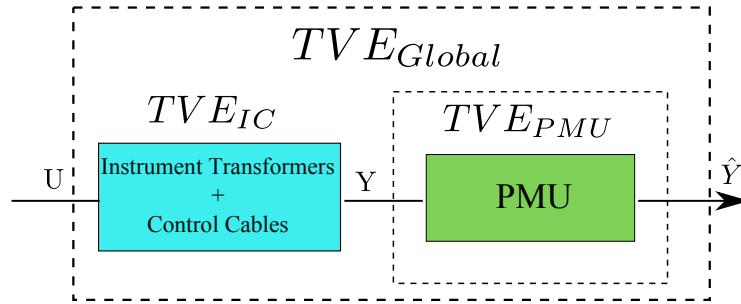


Figure 4.3: The concept of global TVE application

As described in the above sections, phasor estimation process goes beyond just the PMU device and instrumentation channel are known to have a big impact on the phasor quality. With the knowledge of the behaviour of these errors caused by the instrumentation channel, solutions can be developed to compensate for these errors. Similarly, it is necessary to see the effect of the instrumentation channel on timing requirements of PMUs.

5 Assessment of Timing requirements of PMUs: Laboratory Tests

5.1 Introduction

This section presents the tests done in the laboratory to assess the timing requirements of PMUs. A brief introduction of the laboratory test set-up and real-time simulator which was used in the process is also presented.

In order to investigate the effect of the instrumentation channel and assess the timing accuracy required by PMUs, three test scenarios in two different testing arrangements were performed on two commercial PMUs. The first test: Stand-alone Test; results in identification of phase angle errors introduced only by the PMU circuitry itself. The second test method is a real-time Hardware-in-the-Loop (HIL) which facilitates introduction of an instrumentation channel. This helps to realize the contribution of phase angle errors introduced by the IC in the PMU's TVE. Using the same test set-up, in the third test scenario, incremental inaccuracy was imposed in the time source feeding PMU. This step was carried out to investigate how the effect of IC reduces the margin of timing errors for PMUs.

5.2 Stand-alone PMU Test

This test was done on two commercial PMUs which were synchronized using PPS/IRIG-B signals from a GPS based substation clock. The objective of this test was to identify the phase errors caused solely by PMU's sampling, signal processing and estimation circuitry. The test set-up for this test is shown in Fig. 5.1 and in explained below:

As the name suggests, for this test case, the PMUs being tested were not connected to any grid or per say any instrumentation channel. The idea behind this test was to compare the phasor estimated by the PMU under test with a reference phasor estimated by a reference PMU device. The comparison should be done for the same signal measured at same time instant. A stand-alone relay test kit was used to inject voltage signals to the reference PMU and the PMU under test. The reference PMU device used for this purpose was developed on National Instrument's Compact Reconfigurable I/O (NI-cRIO)(hardware) [19] and LabVIEW software [20]. This NI-CRIO PMU has analog input modules for voltage and current signals with 24-bit analog to digital converters and internal clock which could be synchronized using GPS signals with an accuracy in the range of $\pm 1\mu s$. LabView provides the capability to integrate existing software objects to implement an end-to-end measurement and phasor generation system [23].

IEEE Std C37.242-2013 recommends that error associated with PMU testing and

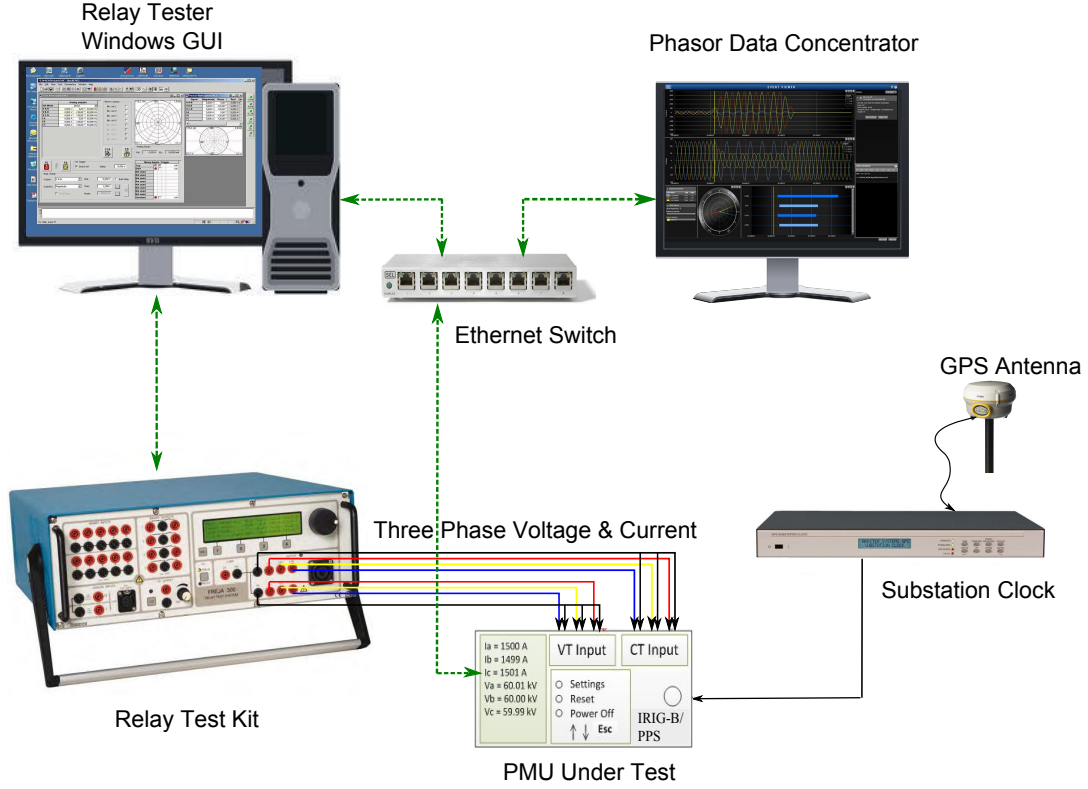


Figure 5.1: PMU test using stand-alone relay test kit

calibration devices should be less than the 10% of the allowed error [3]. For example, if the maximum allowed TVE for PMUs is 1%, then the expected uncertainty of the testing or calibration device should be less than 0.1%. The NI-cRIO used as the reference PMU here was configured to compute reference phasors based on interpolated Discrete Fourier Transform (DFT) synchrophasor estimation algorithm mentioned in [18] with uncertainties two order less than what is required for the PMUs. So this NI-cRIO fits well within the guidelines of [3] to be used as a reference PMU for testing purposes. The cRIO PMU is explained in detail in the following section.

5.2.1 NI-cRIO Reference PMU

NI-cRIO is a reconfigurable embedded controller containing three components: real-time operating system (RTOS) running on a processor, a reconfigurable chassis for Field Programmable Gate Array (FPGA) and various interchangeable input output modules [21]. Fig. 5.2 shows the architecture of the reference PMU consisting NI-cRIO 9076 reconfigurable controller.

The RTOS is able to execute programs in real-time with precision timing and high reliability. It can run reliably for months without stopping. Center of this embedded control system is the reconfigurable I/O FPGA chassis. It facilitates high speed and high performance access to I/O circuitry of each module connected to the

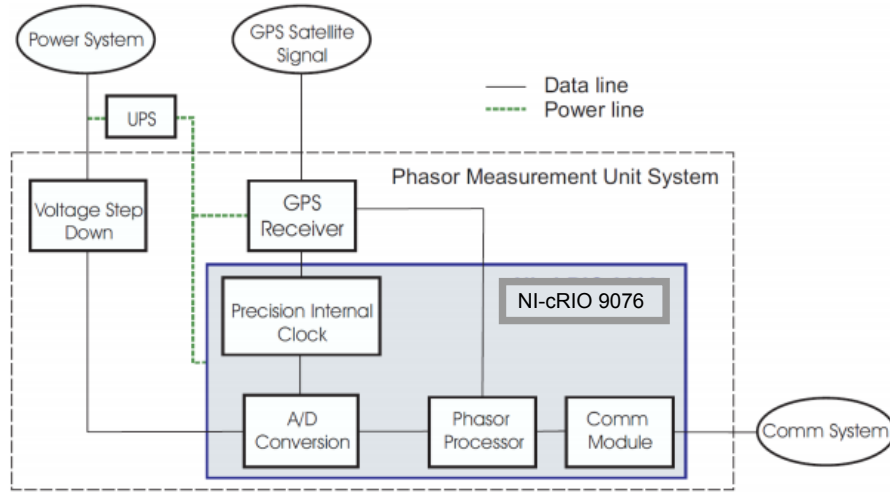


Figure 5.2: Structure of Reference PMU using NI-cRIO 9076 Configurable Controller

chassis via standardized slots. Different modules having different functionalities can be connected to the chassis slots depending upon the requirement. There are many C-series I/O modules for cRIO platform that are designed to meet power system challenges and applications [24]. In this application, the chassis used was NI-cRIO 9076 which has the following configurations [22]

- 400 MHz industrial real-time processor
- 4-slot LX45 FPGA chassis for custom I/O timing, control, and processing
- 10/100BASE-T Ethernet port, USB 2.0 port, and RS232 serial port for connection to peripherals
- Single 9 to 30 VDC power supply input

For acquisition purpose:

- NI 9225 module was used for measuring voltage signals.
- NI 9227 module was used for measuring current signals.
- NI 9467 module was used for GPS synchronization of whole sampling process and the FPGA chassis.

More details about configuring the NI-cRIO 9076 PMU could be found in the appendix.

5.2.2 Relay Test Kit and Procedure

To test the performance of a GPS synchronized PMU in the laboratory, in this stand-alone test, voltage signals are injected in the PMUs using stand-alone relay

test kit called Freja 300 [17] and time was delivered using a high accuracy GPS based substation clock.

Freja-300 is a standard relay testing kit from Megger. Freja-300 can be used with or without a computer. The kit can generate current and voltage signals up to 4 X 150 V (82 VA) and 3 X 15 A (87 VA) or 1 X 45 A (250 VA). The range of error for generation of voltage and current signals is $\pm 0.01\%$ of the range and $\pm 0.05\%$ of the reading) [17]. The allowed TVE for PMUs is $\pm 1\%$, hence the inaccuracy associated with the Freja-300 testing kit is less than 10% of the maximum TVE allowed. This complies with the accuracy requirement set in [3] for the testing and calibration equipments.

For this test three phase voltage signals were injected to the PMU's voltage input terminals. Freja-300's window based Graphical User Interface (GUI) was used from a workstation which is serially connected to the relay test kit. The same voltage signal was sent to the reference PMU with a parallel connection from the same relay test kit. Both the PMUs receive analog inputs and stream out synchrophasor measurements through their Ethernet ports. The synchrophasor measurements are received by the PDC which time aligns all the data received and archive the data as a Comma Separated Value (CSV) file. These CSV files were taken from PDC to for further analysis using MATLAB.

5.2.3 Results

After the analysis of the archived synchrophasor data for detecting phase errors, graphs were plotted to show the results. Figs. 5.3 and 5.4 show the phase angle errors of voltage phasors estimated by PMUs when compared with the reference cRIO PMU. As shown in Fig. 5.3, phase angle errors for PMU 1 are in range of $[0.07^\circ - 0.125^\circ]$. Similarly Fig. 5.4 shows that the phase error for voltage phasors estimated by PMU 2 are in range of $[0.05^\circ - 0.1^\circ]$. As discussed earlier, the major source of these errors are the PMU's signal processing circuitry. However, these errors are well within the limit of 0.573° phase error for which the TVE becomes 1%. Both PMUs when supplied time through GPS comply the TVE requirement set in [4].

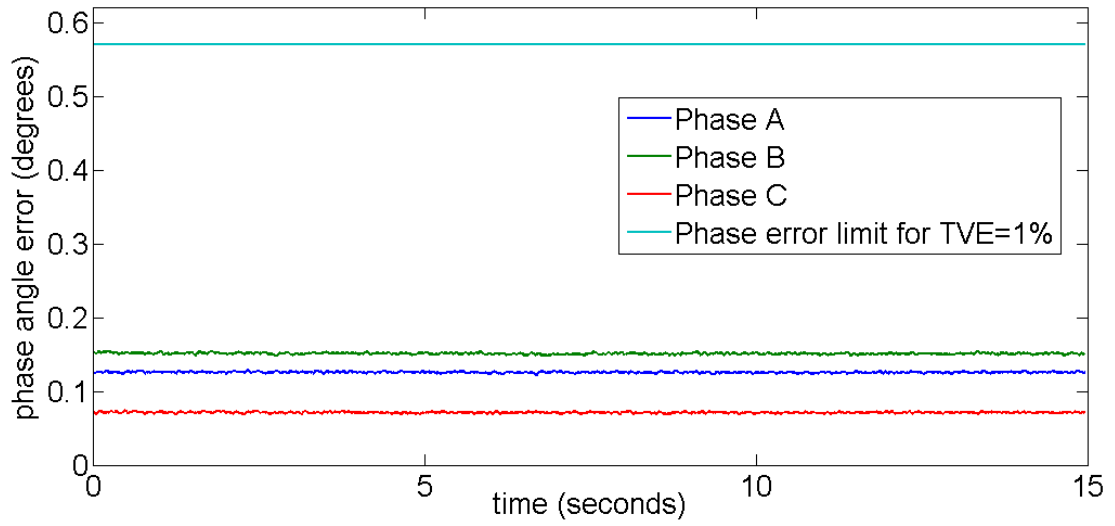


Figure 5.3: PMU1 voltage phase error during stand-alone testing

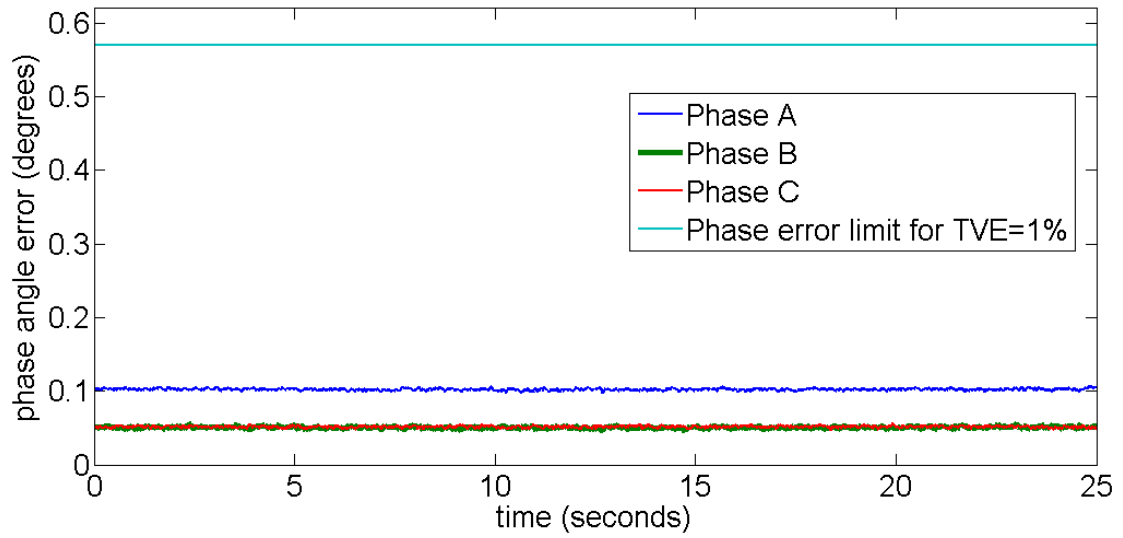


Figure 5.4: PMU2 voltage phase error during stand-alone testing

5.3 Test Set-up 2: Real Time Hardware-in-the-Loop PMU and Instrumentation Channel

As discussed earlier, for fair assessment of timing requirements of PMUs, it is necessary to test the PMU in an environment emulating the on field implementation where, PMU signals are supplied via an instrumentation channel comprising CTs and VTs. The phase errors can be translated directly into time, and hence affect the PMU timing requirements. Hence, test case 2 investigates the phase angle errors for phasors calculated by PMUs which are receiving input signals from CTs and VTs. Effect of different timing inaccuracies on the phase error was studied in test case 3 but using the same test set-up.

To see the effect of varying timing errors on the TVE and hence estimate the acceptable accuracy limits of the timing source, a controllable PMU timing solution is required. This timing solution would be able to supply time with varying accuracy. In the previously discussed stand-alone test, there is no instrumentation channel. The time clock supplying the time to PMU is assisted by GPS and hence is uncontrollable. The test set-up discussed in subsequent subsections tests the PMUs in presence of an emulated instrumentation channel and using a user controllable time source whose accuracy can be varied as and when required in real-time.

To emulate the instrumentation channel, single phase SMRT1 amplifiers from Megger were used in between the current or voltage signals generation source and the PMU under test [25]. For these Megger amplifiers, the phase angle accuracy of the output current or voltage signals was in the range of to $\pm 0.25^\circ$ at 50 Hz [25]. The phase angle accuracy of these amplifiers range was found comparable with that of Instrumentation channel comprising all of its components. This made these Megger amplifiers suitable to be used to emulate an IC.

To be able to control the PMU timing signal, it was decided to use the Simulink platform to simulate a time signal and execute the model in real-time to feed the PMUs. Basic control blocks from Simulink's library can be used to vary the accuracy of the time signal supplied. For its high accuracy, and reliability, unmodulated, DC-shifted, IRIG-B timing signals were chose to supply time to PMUs.

After the basic introduction of IRIG-B in Section 3.2, a more detailed structure of IRIG-B time code which was simulated in real-time to distribute time to PMUs under test is briefly discussed below.

5.3.1 IRIG-B Code Overview

IRIG-B is a serial time code developed by the Telecommunication Group of IRIG. IRIG has six different encoding formats labelled A, B, D, E, G and H, out of which IRIG-B is most commonly used to distribute time to IEDs [7]. IRIG-B can be distributed in two ways, one as a DC Level Shifted (DCLS) pulse width coded signal

(unmodulated) or as an amplitude modulated signal based on a sine wave carrier with a frequency of 1kHz. GPS based clocks can generate IRIG-B coded timing signals which can be distributed to many IEDs in a single substation. Unmodulated DCLS IRIG-B can achieve accuracies in the range of ± 500 ns, which is better than the accuracy of $\pm 10 \mu s$ achievable by its amplitude modulated counterpart [26]. This makes the DC shifted, unmodulated form of IRIG-B the most suitable format for time distribution in PMU applications.

5.3.2 Unmodulated DCLS IRIG-B

Unmodulated DCLS IRIG-B is distributed in frames. Each frame is one second long and has a pulse rate (or a bit rate) of 100 pulses per second (pps). The *on-time* for each bit refers to the leading edge of the pulse. Each bit has an *index count* identification number. The *index count interval* is the time interval between the leading edges of two consecutive pulses. Each bit has an index interval of 10 ms [26]. The index count ranges from 0 to 99 and then rolls over to 0 for the next second. Each frame uses five types of pulses: logic zero, logic one, position markers $P_0 - P_9$, a reference bit P_r and index markers. Reference bit P_r indicates start of a new frame. Position identifiers from P_0 through P_9 are placed every ten bits. Index markers occur between decimal digits in each sub-word to provide visual separation. The width of these pulses are pulse width coded where the width of logic zero is set to be 20% of the index interval (2 ms), the width of logic one is 50% of the index interval (5 ms). Position markers and the reference bit are 80% of the index interval (8 ms) and index marker bits are 20% of the index interval (2 ms). Every new one-second time frame is identified by two consecutive 8 ms pulses, P_0 and P_r . The structure of an IRIG-B frame is presented below:

$\langle \text{synch} \rangle SS:MM:HH:DDD \langle \text{Control} \rangle \langle \text{Binary Seconds} \rangle$

where:

<i>SS</i>	The second of the minute [00 to 59 (60 during leap seconds)] in Binary Coded Decimal (BCD)
<i>MM</i>	The minute of the hour (00 to 59) in BCD
<i>HH</i>	The hour of day (00 to 23) in BCD
<i>DDD</i>	The day of year (001 to 366) in BCD
<i>Control</i>	Informations like leap second, daylight saving, quality information and a parity bit included in a block of 27 bits
<i>Binary Seconds</i>	Second of the day in 17 bits



To be able to use IRIG-B as a controllable timing source for PMUs under test, MATLAB code was written to generate pulse width modulated IRIG-B signals in the DCLS format as shown in Fig. 5.5. The code was embedded in a Simulink model as a MATLAB function. The code includes an option to set the initial time from which time starts rolling. Other control parameters like daylight saving, leap seconds and time quality can also be set and changed. The parameters giving initial time of the IRIG-B time block can be set as shown in Fig. 5.6.

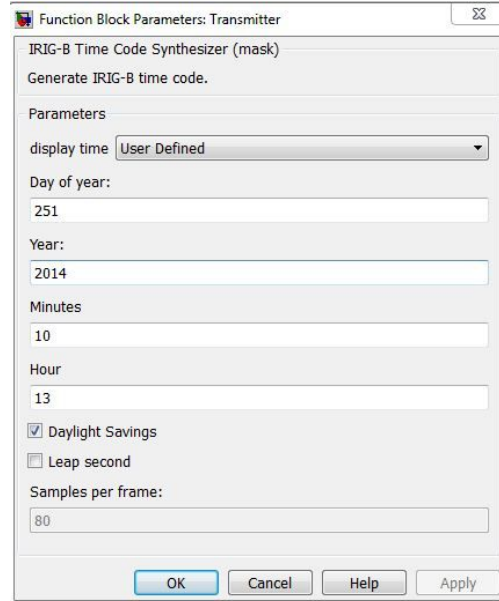


Figure 5.6: Initial parameters for IRIG-B generator block in SIMULINK

Along with the IRIG-B time code, the required three phase voltage and current signals were also simulated in Simulink. All these signals use the same time as reference and were executed in the real-time on Opal-RT's eMEGASIM real-time simulator [28]. The simulator has analog-out channels from where real-time analog IRIG-B pulses and sinusoidal voltage and current signals were taken out. The voltage and current signals were feed to the PMUs via the emulated instrumentation channel. More details about the real-time simulator used in this set-up can be found in the appendix.

IRIG-B time code pulses of 5.5V amplitude generated in real-time were directly sent to the PMU IRIG-B input. This synchronized the PMUs to the time specified by the initial parameters set by the user. The three phase voltage and current signals generated by the simulator were amplified using the Megger SMRT1 amplifiers and then were fed to the voltage and current inputs of the PMU.

In this set-up, the Megger amplifiers emulated on-field CTs and VTs as they similarly introduce phase angle shifts in the voltage and current signals. The whole channel from the real-time simulator's output to the PMU's current and voltage inputs including the amplifiers and the connection cables represents the instrumen-

tation channel. The complete model-to-data analysis work-flow for this test is shown in Fig. 5.7. The green lines in the figure indicate transfer of data over Ethernet. The instrument channel is shown using the red arrows. The analog outputs retrieved from the simulator in real-time is shown in the Fig. 5.8

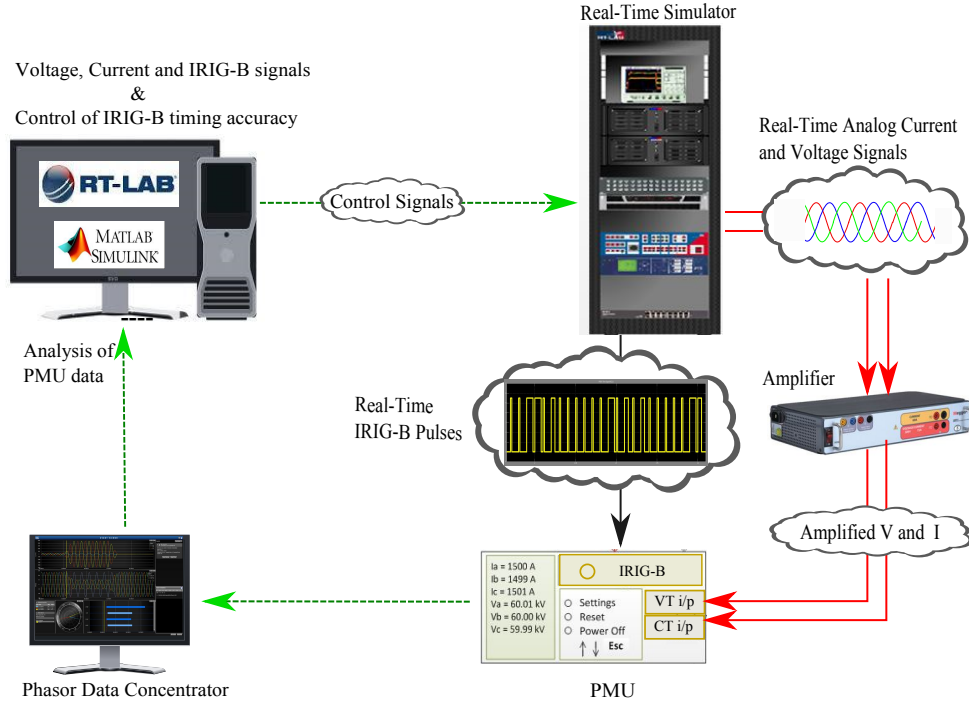


Figure 5.7: Real-Time, Hardware-in-the-loop set-up to determine timing accuracy requirements

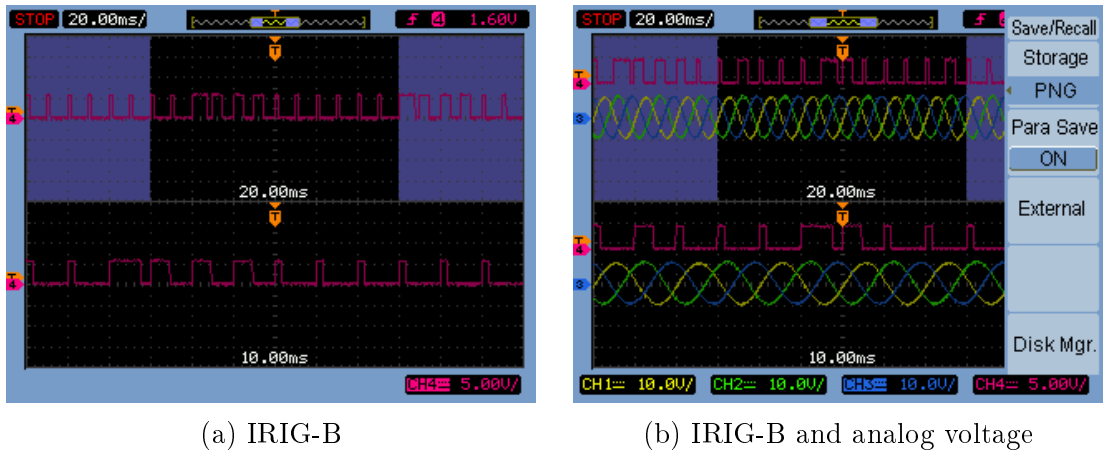


Figure 5.8: Oscilloscope view of the real-time simulation of analog IIRIG-B and voltage signals acquired from the Simulator's output ports. The time reference for both the signals is same.

The PMU makes phasor estimates of the signals received. The timing signals can be manipulated by the user during the test. Basic blocks like *Transmission Delay* from Simulink's library can be used to delay the time signals for a few microseconds to a few milliseconds. In the experiment, the time errors were varied in the steps of $10\ \mu\text{s}$. Continuously generated synchrophasor estimates by the PMU for different timing errors were sent to the Phasor Data Concentrator (PDC) and stored. This logged data was analysed using MATLAB. The effect of timing errors on the phase errors of the measured signals and consequently on the overall TVE of the estimated phasor is presented in the following section.

5.3.3 Results

This section will present the results from the real-time HIL tests conducted as explained earlier. The results are presented in two sections. Section I (test case 2) presents the results of the real-time HIL tests where PMU was supplied voltage and current signals via an instrumentation channel. The PMU synchronization was achieved by feeding IRIG-B time signals received from the output channels of the real-time simulator. There was no time inaccuracies imposed on the timing signals by the user in this case. Section II presents results from the tests where timing inaccuracies were introduced in the PMU synchronization by manipulating the delivery of IRIG-B time code in real-time.

Section I (Test Case 2)

Figures 5.9 and 5.10 show the plots of voltage and current phase errors when the PMU was synchronized using simulated IRIG-B and no deliberate timing inaccuracy was imposed. Although the time distributed was accurate up to $\pm 500\text{ns}$ (accuracy range of IRIG-B), the voltage phase angle errors were observed in the range of $[0.332^\circ\text{-}0.46^\circ]$ for PMU1 and $[0.32^\circ\text{-}0.45^\circ]$ for PMU2. So, the voltage phase angle errors for both PMUs increased by a factor of 5-7 times just by the inclusion of the IC.

Phase angle errors for current signals were observed in the range of *negative* $[0.187^\circ\text{-}0.465^\circ]$ for PMU1 and *negative* $[0.240^\circ\text{-}0.494^\circ]$ for PMU2. This is due to the phase angle shift caused by the CTs and VTs inside the amplifiers which are emulating the on-field CTs and VTs. As mentioned earlier, the voltage signal output from the VT lags the original signal and the output current signal from the CT leads the original current signal. For notational purpose, keeping the original phase as reference, the lagging phase error is assumed to be positive and the leading phase error is assumed to be negative.

In this test scenario, the results show that, even though the errors are still under 0.573° limit, there is very little margin left for errors due to timing inaccuracies. Depending upon the phase errors associated with CTs and VTs used in the experiment, the TVE of a PMU could have broken the limit of 1% even when it is synchronized by a timing source with sub-microsecond accuracy.

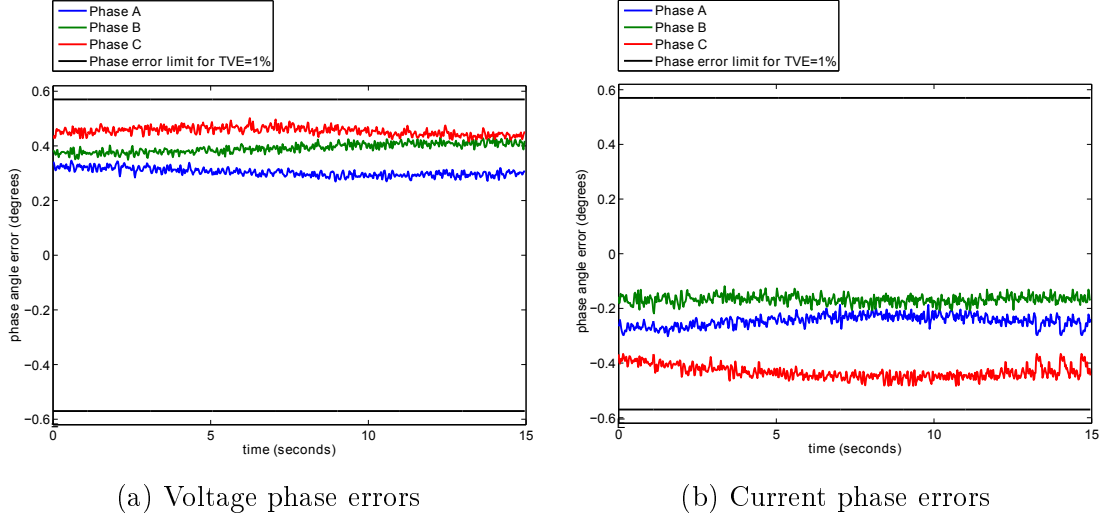


Figure 5.9: Phase errors in PMU 1 phasor estimates in presence of an instrumentation channel.

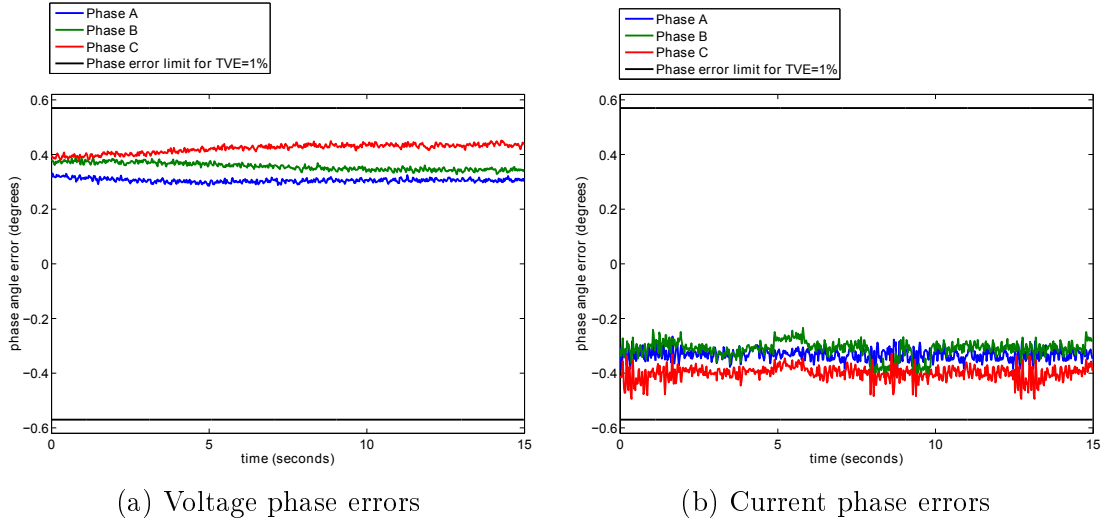


Figure 5.10: Phase errors in PMU 1 phasor estimates in presence of an instrumentation channel.

Section II (Test Case 3)

This section presents results of tests on PMUs when their timing was manipulated in real-time. To be able to vary the accuracy of PMU timing, controlled time errors were imposed in the real-time simulation of IRIG-B signal being supplied to the PMUs. Starting with zero error, the errors were imposed in successive steps of $10\mu\text{s}$ at the points in time marked by A, B, C, D and E in Figs. 5.12 to 5.15. At each step the error in timing was raised by $10\mu\text{s}$. The effect of time errors was evaluated for two different scenarios : leading i.e. supplied time advancing ahead of the correct time and lagging i.e. supplied time lagging the correct time. The phase angle errors

were analysed from the stored data.

It should be noted that varying the time error in the IRIG-B signal, caused the PMU to give unstable and incorrect phasor estimates for a few seconds before settling down. Although PMUs are capable of handling some amount of jitters in the timing signals but a jitter of $10\ \mu\text{s}$ was enough to force the PMU out of synchronization for some time. Although, interestingly, the PMU continues to estimate and transmit erroneous phasors to the PDC. The erroneous phasor signals have been filtered and are not included in the figures. However, for demonstration purpose, Fig. 5.11 shows the transient duration while the PMU 1 settles down to the new time.

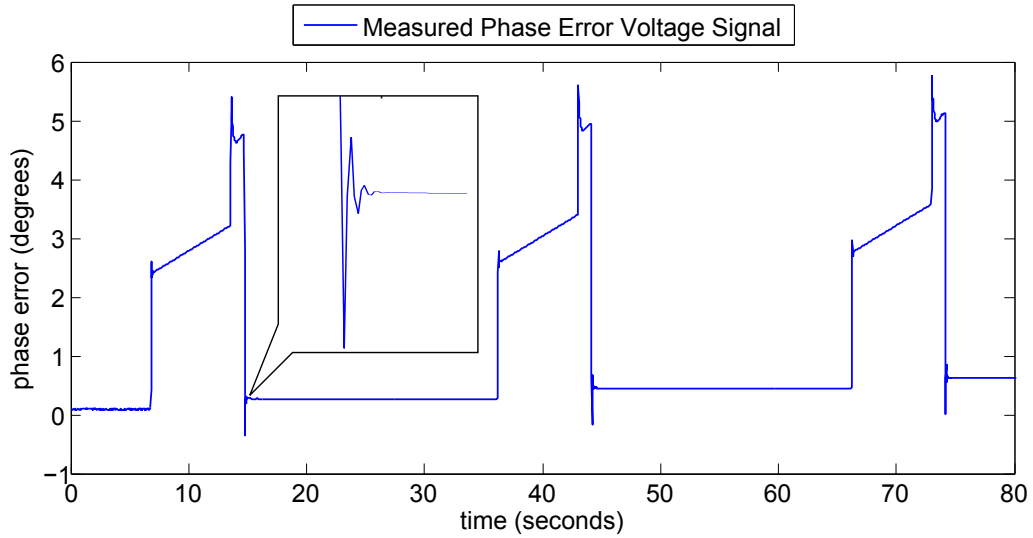


Figure 5.11: Voltage phase errors calculated from the synchrophasor data sent by PMU 1. Transient in the phase errors can be seen when the accuracy of IRIG-B changes and the PMU takes time to settle down to the new time. Meanwhile the PMU keep streaming the incorrect phasors.

Figs. 5.12a and 5.12b show the effect of leading time error in steps of $10\ \mu\text{s}$ on the voltage and current phase errors respectively for PMU 1. Since the voltage input to the PMU were already lagging the actual voltage due to the phase errors introduced by the VTs, the leading time error of PMUs's clock increases the phase error in the estimated phasor. **Thus, with an increased phase error due to the effect of VTs, the TVE touches the 1% mark for one of the voltage phases only after a $10\ \mu\text{s}$ error in PMU timing and the TVE crosses the 1% mark for all the phases by a total timing error of $20\ \mu\text{s}$, which is much lower than the $31.6\ \mu\text{s}$ limit set in [4].**

The current phasors show a different behaviour. As shown in Fig. 5.12b, introducing a leading time error initially causes the measured phase error to decrease. As the timing error was further increased the measured phase error crosses zero and starts to increase in the opposite direction. This is due to the fact that the current phasor input to the PMU was leading the original signal's phasor due to the effect

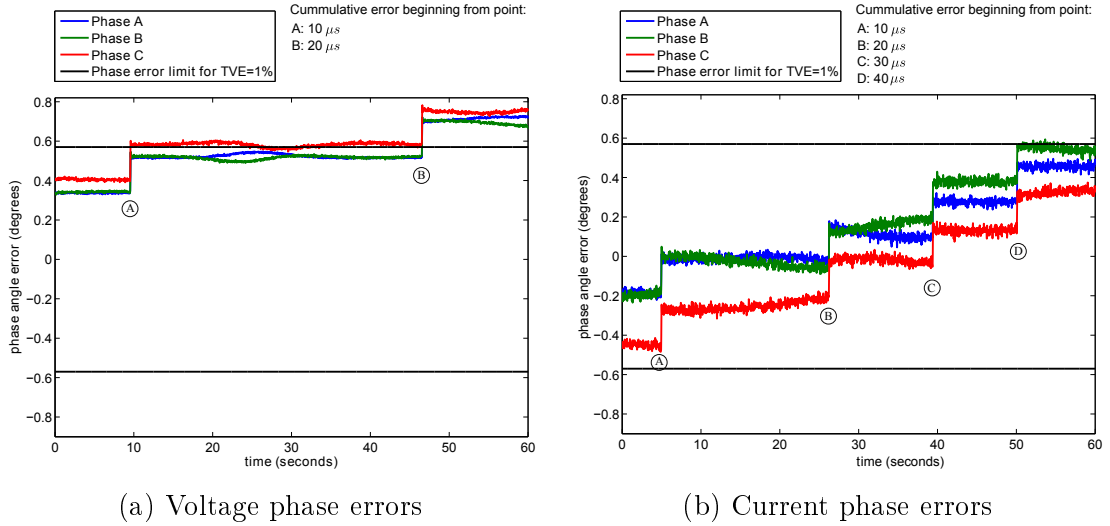


Figure 5.12: Effect of increasing time inaccuracies in terms of a *time lead error* on phase errors of PMU 1 in presence of an instrumentation channel.

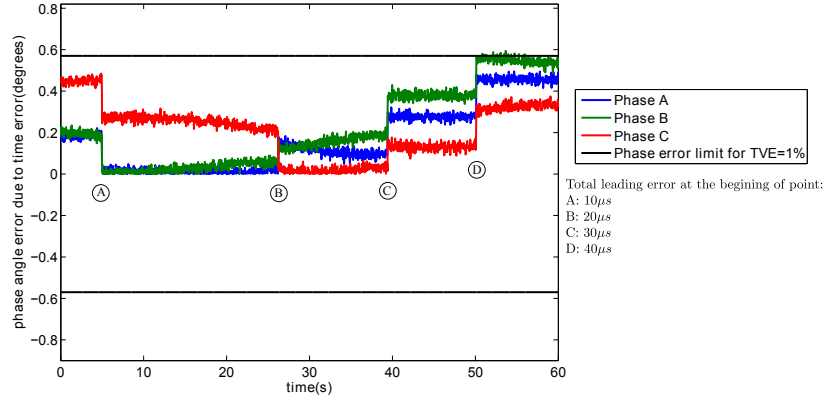


Figure 5.13: Absolute phase errors in current phasors by PMU2 due to *time lead error* in presence of an instrumentation channel

of the phase error introduced by CTs. So when the time is erroneously advanced, up to a certain magnitude of timing error, the effect of leading timing error decreases the effect of the leading phase error and the PMU makes a better phasor estimate of the current phasor. At a certain leading time error, its effect completely cancels out the effect of error in phase caused by the CTs. Afterwards, any increase in leading timing error, results in an increase in the measured phase error but in opposite direction. The phase angle error will start to increase again but in opposite direction.

This phenomena is also depicted in Fig. 5.13, where the absolute value of the phase errors were plotted. As described earlier, the phase error initially decreases upto a certain timing error before increasing again.

In the next step, lagging timing errors were imposed on PMU 1 by delaying the time in successive steps of $10\mu s$. The effects on the phase errors of voltage and current can be seen in Figs. 5.14a and 5.14b. As shown in Fig. 5.14a, as the lagging timing error increases, the voltage phase error decreases and increases in the negative direction. This is due to the fact that the voltage signals that feed the PMU via VTs lag the original voltage signals, therefore when the time is delayed, the measured phase error starts decreasing first towards zero and then subsequently increasing in the negative direction. However, as shown in Fig. 5.14b, the measured phase error of the current signal increases in the negative direction resulting in one of the phases crossing the phase error limit at a time delay error of $10\mu s$. With total delay error of $20\mu s$ all the phases had crossed the 1% TVE phase error limit. Both the time errors were much lower than the $31.6\mu s$ limit set in [4].

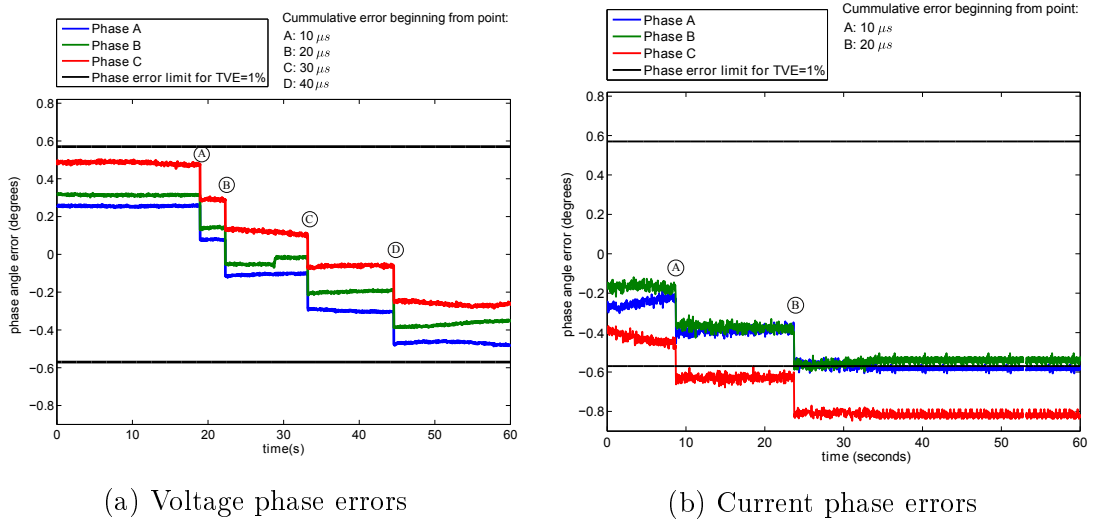


Figure 5.14: Effect of increasing time inaccuracies in terms of a *time lag error* on phase errors of PMU 1 in presence of an instrumentation channel

As discussed, both of the above mentioned time error scenarios (leading and lagging), measured phase errors of either the current or the **voltage signals violate the 1% TVE rule even before the timing error reaches the $31.8\mu s$ limit, set in [4].**

A similar set of tests were repeated for PMU 2. Fig. 5.15 display the measured phase errors in the case of lagging timing errors for PMU 2. When lagging time errors were imposed on PMU 2 timing signal, its effect on the phase errors was also similar to that of PMU 1. So, as seen in Fig. 5.15a, the voltage phase errors tends to decrease as delayed time aligns the input voltage better with the actual voltage phasor cancelling the delay effect of the VTs. Eventually this phase error increases in opposite direction. For current phasors, the phase errors start to increase from the first time delay as was the case for PMU 1.

All the results indicate that PMUs require a time source with a better

accuracy than the $31.8\mu s$ limit set in [4]. These results also confirm that in order to limit the TVE of PMUs below 1%, high accuracy time synchronization methods such as GPS, IRIG-B and hardware supported PTP with sub-microsecond accuracy are required.

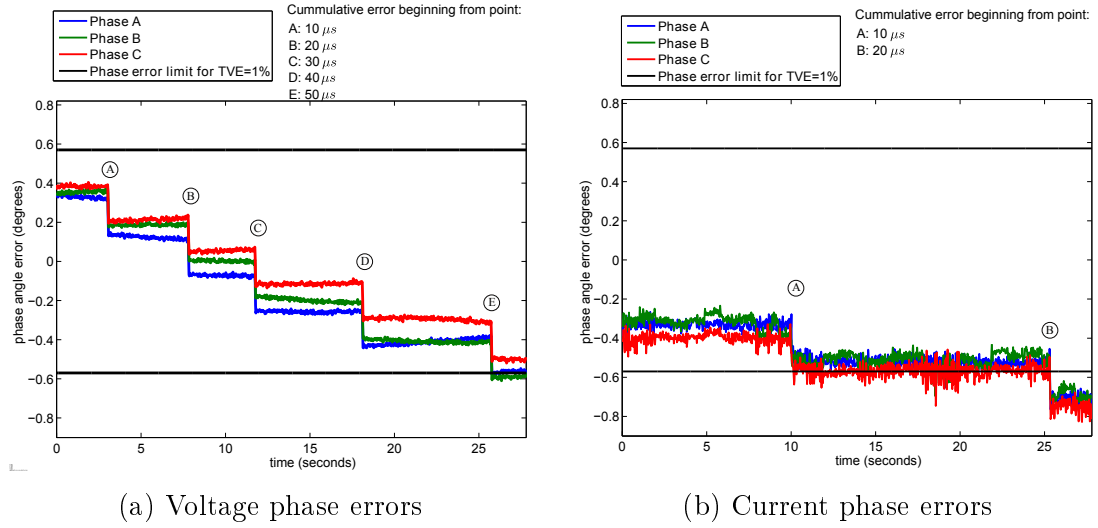


Figure 5.15: Effect of increasing time inaccuracies in terms of a *time lag error* on phase errors of PMU 2 in presence of an instrumentation channel

6 Closure

6.1 Summary and Conclusion

The initial part of the thesis discussed different sources and distribution methods to provide timing solutions to IEDs and compared their usability as time sources for PMU time synchronization. It was concluded that GPS, hardware assisted PTP and IRIG-B are capable time synchronization solutions for PMU applications. To further investigate the timing requirements of PMUs, two commercial PMUs were tested for their TVEs caused by phase errors as a result of timing inaccuracies using a real-time HIL test set-up. This set-up also used amplifiers to emulate CTs and VTs of the instrumentation channel. A high-accuracy version of IRIG-B time signal was coded successfully to feed high-accuracy time to the PMUs in the laboratory. The tests were performed using a controlled simulation of this IRIG-B timing code to explore the effects of timing errors on the TVE.

It was shown that for two different commercial PMUs that the final phasor measurement error could be quite large due to its instrumentation channel. These factors of TVE errors affect the accuracy of the PMU measurements and will also make the timing requirements more stringent. Thus, PMU timing accuracy requirements need to be evaluated while keeping the effects of instrumentation channel errors in consideration. The tests showed that even a time source error of $10\mu s$ could be sufficient to make TVE higher than 1%. It is concluded that to leave some margin for other errors, the required timing source accuracy should be well in sub-microsecond range. It was also observed that PMUs could keep on transmitting faulty phasor data during jitters in timing signals. This type of bad data could be disastrous for any control algorithm utilizing PMU's data. Insight about errors like this could be useful for applications where bad data screening is an important requisite.

6.2 Future Work

The importance of accurate time synchronization in synchrophasor applications makes it important to assess the effect of time synchronization errors on the operation of such applications. For applications which use phasor angles for their operation, this assessment becomes most important as timing errors directly affect the estimation of phase angles of the signals.

After the assessment of the impact caused by timing errors, if the application requires, methods could be formulated to condition the data in real-time before feeding it to the application.

In near future, different timing solutions will be available for synchrophasor applications making it possible to synchronize a single device unit using multiple time sources. More work could be done to develop an intelligent algorithm which allows the device to choose the best timing option in real-time and build redundancy for

accurate timing. The insight about time synchronization effects could also help in selection timing source for different applications. More studies in an laboratory set-up could be done in all these regards.

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A Setting-Up NI-Crio 9076 as a reference PMU

To set up the reference PMU, three different modules from NI were utilized and placed in NI-9076 slots:

- Slot 1: NI 9225 Voltage measurement module.
 - 50 kS/s/ch simultaneous inputs
 - Built-in anti-aliasing filters
 - 300 Vrms measurement range
- Slot 2: NI 9227 Current measurement module.
 - 50 kS/s/ch simultaneous inputs
 - Built-in anti-aliasing filters
 - 5 Arms measurement range
- Slot 4: NI 9467 GPS synchronization module.

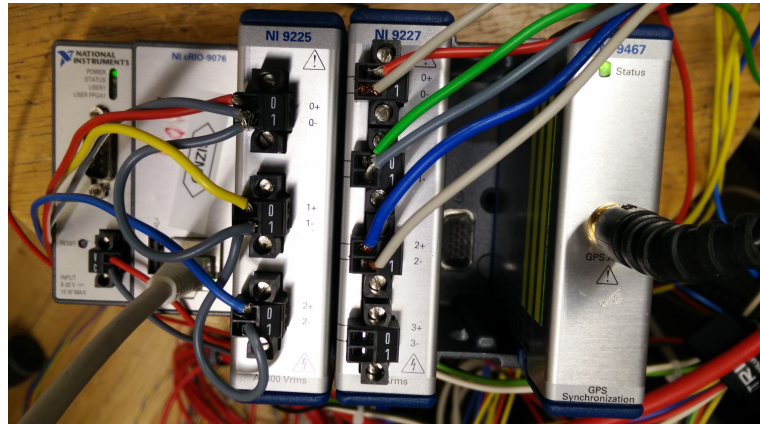


Figure A.1: cRIO PMU with required modules and wire connections

Three phase wiring was done as shown in Fig. A.1. A 5 V active antenna input is provided to the module NI 9467. PMU is connected to the network using a standard Ethernet cable plugged in the Ethernet port. Using the cRIOs web interface, the device is set to be used as a PMU by setting its communication parameter, selecting the phasors it will stream out. The measured signals and phasors being sent to the PDC can be monitored over the same web based interface. Figures A.2 and to A.4 show the web-interface for cRIO which could be used for setting up the PMU parameters, choosing phasors to transmit and monitoring the analog values and phasors.

Configuration | Scope | Data Frame | Diagnostics

Base Config | Sensors | Phasors | Analog | Advanced Settings

nominal frequency: 60 Hz
reporting rate: 30 S/s

station name: PMU
header: NI PMU
PMU ID: 1

Communication Settings:

Channel 1	Channel 2
communication protocol: TCP	communication protocol: Disable
TCP port: 4712	TCP port: 4714
UDP port: 4713	UDP port: 4715
UDP remote host:	UDP remote host:

Update Config

Figure A.2: Setting of communication parameters on NI-9076 PMU

Configuration | Scope | Data Frame | Diagnostics

Base Config | Sensors | Phasors | Analog | Advanced Settings

Positive Sequence Voltage: ☒ V+
Positive Sequence Current: ☐ I+
Negative Sequence Voltage: ☐ V-
Negative Sequence Current: ☐ I-
Zero Sequence Voltage: ☐ V0
Zero Sequence Current: ☐ I0

Va: ☒ Va
Ia: ☐ Ia
Vb: ☐ Vb
Ib: ☐ Ib
Vc: ☒ Vc
Ic: ☐ Ic

Update Config

Figure A.3: Selecting phasors to stream over to PDC

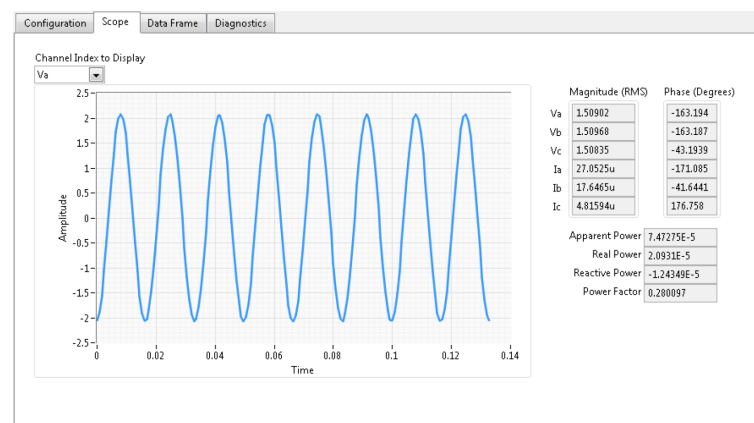


Figure A.4: Monitoring the phasors measured by the cRIO PMU on its web interface

B Real-Time Simulator and PDC

The core of the real-time test set-up was the real-time simulator from Opal-RT. The simulator is an embedded system consisting a powerful ‘target’ computer along with high-speed FPGA board to manage analog and/or digital I/Os, various signal processing modules and communication and networking interfaces [28]. The target computer runs a Linux based real-time operating system on its 12-cores with 3.3 GHz Intel i7 processors [28]. Models created in MATLAB/Simulink can be loaded on the simulator to be run in real-time. The simulator can interact with other devices through its low power analog/digital outputs using standard connectors at the front and back. It can also stream data over TCP/IP or UDP. There are various other additional capabilities and functionalities of Opal-RT’s simulator not mentioned here which can be found out in the product description manual [28]

For this work, the simulator was used for real-time simulation of IRIG-B signals along with the current and voltage signals. Use of Opal-RT’s RT-LAB enabled the Simulink model to run in real-time on the simulator [29]. To develop real-time executable models using RT-LAB, the top level of the Simulink model should only have *subsystems*. Each subsystem is run on individual cores of the simulator. Some additional blocks from RT-LAB were used in the Simulink models to help the model interact with hardware in real-time. For example:

OpCtrl and Analog Out Blocks- OpCtrl programs the FPGA board, initialize it, selects the synchronization mode. Analog Out facilitates input and output of signals by configuring I/O blocks

OpComm Block- Facilitates synchronous communication between the two subsystems running on different cores or asynchronous communication between the user computer and a subsystem running on a core.

Fig. B.1 shows a Simulink model created in RT-LAB to simulate real-time voltage and current signals.

The PDC and its associated software were from Schweitzer Engineering Laboratories (SEL). The PDC runs on a computer with windows operating system and a big hard-disk space for archiving the synchrophasor streams. Synchrophasor data streams from the PMUs under test and the reference NI-cRIO were added to the PDC using its windows interface. New output streams were created which would transit the time-aligned synchrophasor data from PDC computer to user computer over TCP.

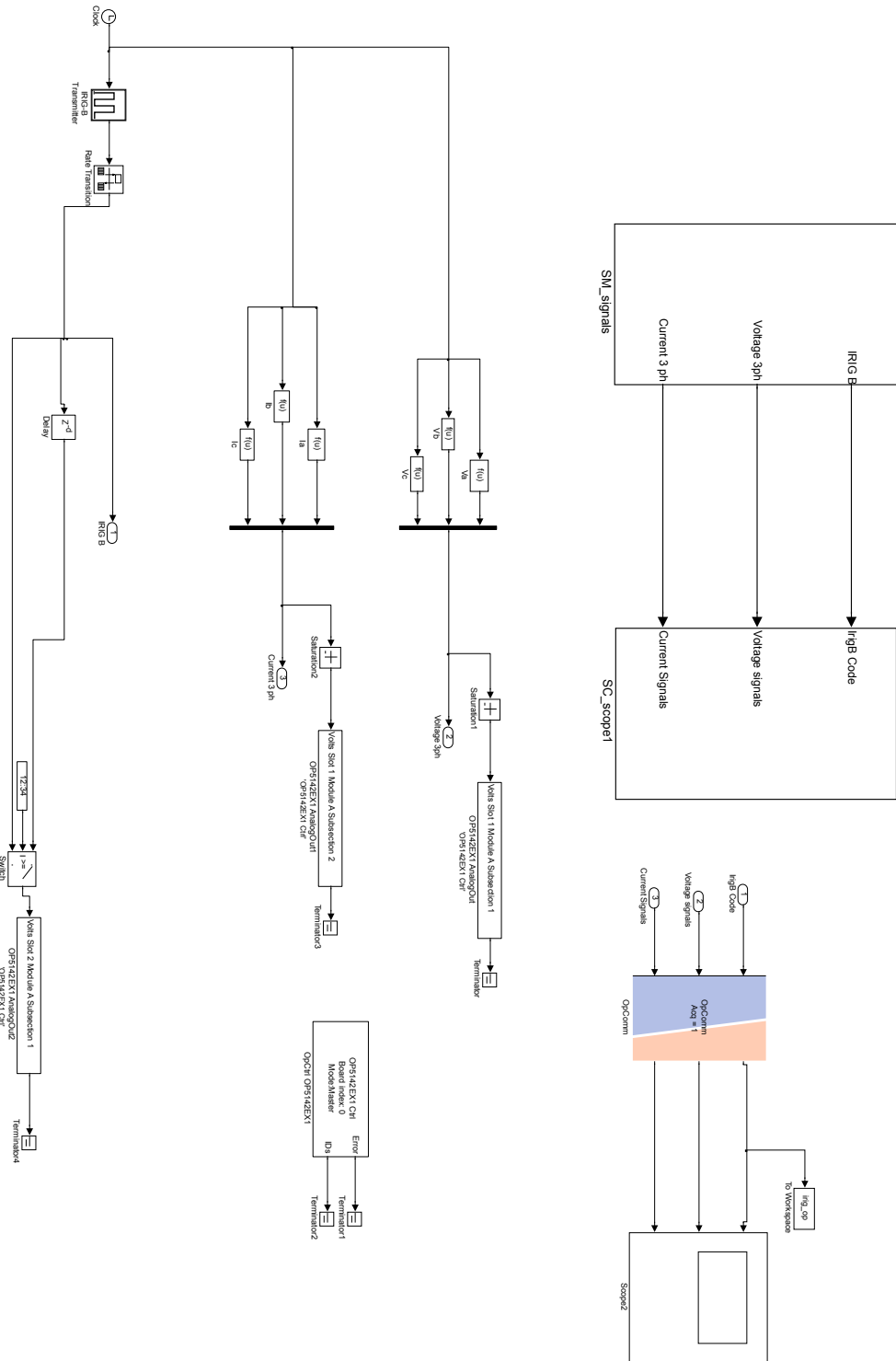
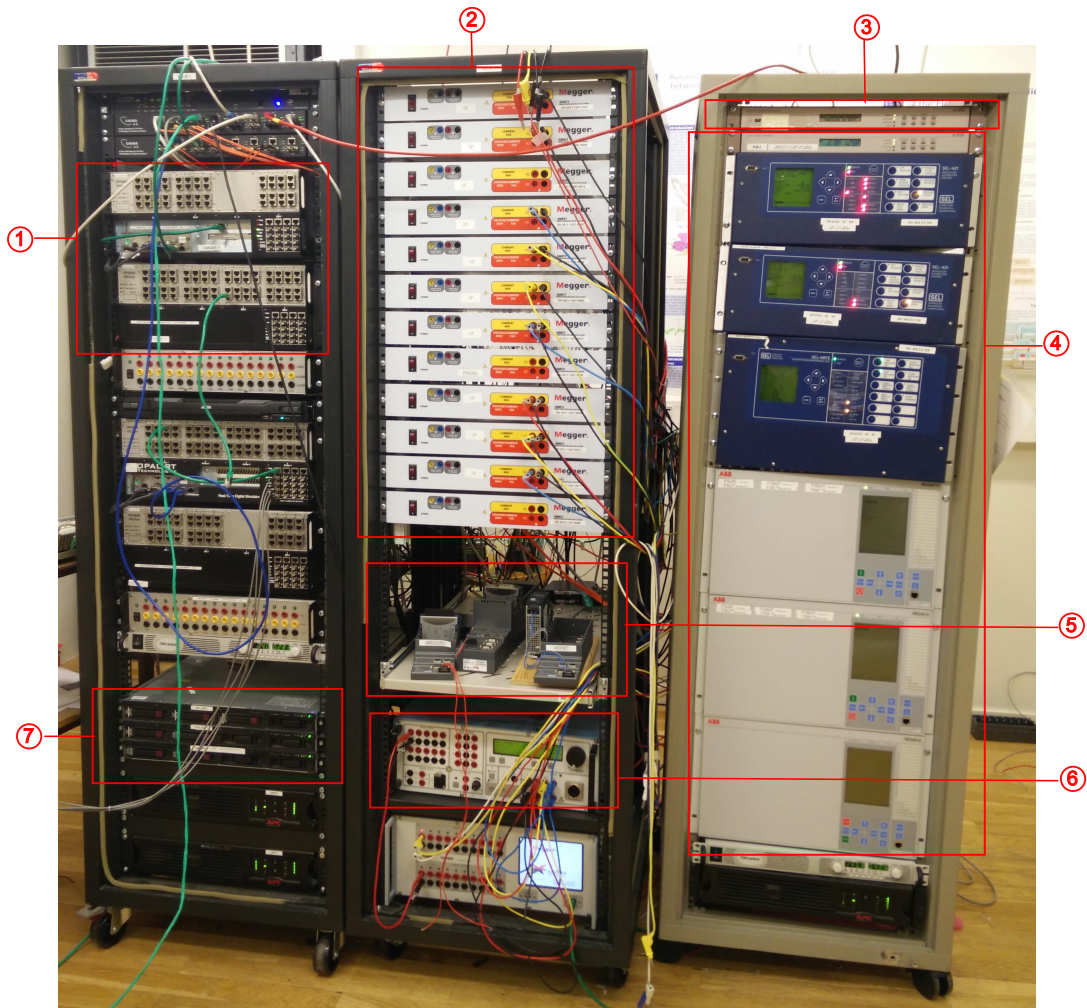


Figure B.1: A simulink model created in RT-LAB to simulate IRIG-B, voltage and current signals. OpCtrl OP5142EX1 and OP5142EX1 AnalogOut blocks are the OpCtrl and Analog Out blocks associated with the FPGA board named *OP5142* present in the simulator.



- | | |
|------------------------------------|-----------------------------|
| 1. Real-time Simulator | 5. NI-cRIO as Reference PMU |
| 2. Voltage and Current Amplifiers | 6. Relay Testing Kit |
| 3. Substation Clock | 7. PDC Servers |
| 4. Relays with PMU functionalities | |

Figure B.2: This figure shows the set-up of equipment used through out this thesis work for testing the PMUs at SmarTS lab, KTH.

C IRIG-B Simulation Code

```

function y2 = gen_irig_PWM_symbols(mode, hr,mints, day, yr, dst,leap, sec)

persistent y idxSymbol idxSimFrame SimFramesPerSymbol

% Constants
IRIGSymbols = 100;

SimFramesPerSymbol = 100;
NumSymbols = IRIGSymbols;

% Initialize persistent variables
% Initialize symbols vector
if isempty(y), y = zeros(NumSymbols,1); end
% Initialize counter for symbols (goes from 1 to NumSymbols)
if isempty(idxSymbol), idxSymbol = 1; end
% Initialize counter for Simulation frame. For each symbol, the number of
% Size of each frame is 1 samples.
if isempty(idxSimFrame), idxSimFrame = 1; end
% Initialize number of simulation frames per symbol to SimFramesPerSymbol;
if isempty(SimFramesPerSymbol), SimFramesPerSymbol = 100; end

if (idxSymbol == 1) && (idxSimFrame == 1)

    x = struct('yr',0,'leap',false,'utc',0,'ut1',0,'day',0,'dst',false,
        'dst2',false,'mints',0,'sec',0,'hr',0);

    x.sec    = rem(floor(sec),60); % seconds add remainder function
    x.mints  = rem((mints+floor(sec/60)),60); % minutes
    x.hr     = rem((hr+floor(sec/3600)),24); % hours

    x.day    = day; % day of year
    x.yr     = yr; % year
    x.dst    = logical(dst); % Daylight Savings Time indicator
    x.leap   = logical(leap); % Leap second

    % Generate symbol vector:
    y = gen_irig(x);

end

%Generate modulated tone by doing Pulse width modulation on the WWV symbols.
%Generate NumSimFramesPerSymbol number of simulink frames for each symbol.
y2 = zeros(1,1);
if (idxSimFrame <= SimFramesPerSymbol)
    y2 = gen_tone(y(idxSymbol),idxSimFrame);
end

```

```

idxSimFrame = idxSimFrame+1;
if (idxSimFrame > SimFramesPerSymbol)
    idxSimFrame = 1;
    idxSymbol = idxSymbol+1;
    if (idxSymbol > NumSymbols)
        idxSymbol = 1;
    end
end

function s = gen_tone(x,whichSimFrame)

P0    =1; % logic 0
P1    =2; % logic 1
PMARK=3; % marker

cs=5.5; % output voltage amplitude
s = zeros(1,1);

switch x
    case P0,
        if (whichSimFrame <= 17)
            s = cs;
        end
    case P1,
        if (whichSimFrame <= 47)
            s = cs;
        end
    case PMARK,
        if (whichSimFrame <= 77)
            s = cs;
        end
    otherwise,
end

return

% =====

function y = gen_irig(x)

P0    = 1;
P1    = 2;
PMARK = 3;

% Preload with all P0's:
% -----
y = P0*ones(100,1);

% 10-sec markers:
% -----

```

```

y(10:10:end) = PMARK;

% Start-of-frame marker:
% -----
y(1) = PMARK;

% Data:
% -----
ybcd = bcd(x.yr-1900,2); %year
y(51:54) = fliplr(ybcd(1:4));
y(56:59) = fliplr(ybcd(5:8));

ss=bcd(x.sec,2); %seconds
y(2:5) = fliplr(ss(1:4));
y(7:9) = fliplr(ss(6:8));

hh = floor(x.hr); %hours
hbcd=bcd(hh,2);
mm = x.mints; %minutes
mbcd = bcd(mm,2);
y(11:14) = fliplr(mbcd(1:4));
y(16:18) = fliplr(mbcd(6:8));
y(21:24) = fliplr(hbcd(1:4));
y(26:27) = fliplr(hbcd(7:8));

ybcda = bcd(x.day,3); %day
y(31:34) = fliplr(ybcda(1:4));
y(36:39) = fliplr(ybcda(5:8));
y(41:42) = fliplr(ybcda(11:12));

% Control Bits (refer IRIG-B code details for more information)
% http://www.irigb.com/pdf/wp-irig-200-98.pdf
% -----
y(61:63) = P0;
y(64) = bit(x.dst);
y(65) =P0;
ybcdb = bcd(abs(x.ut1*10),1);
y(66:69) = fliplr(ybcdb(1:4));
y(71) =P0;
y(72:75) =P0;

% -----
% y(76) is a parity bit, so for loop to evaluate the value of parity bit:
j=0;
for i=1:75
    if isequal(y(i),2)==1
        j=j+1;
    else
        j=j;
    end
end
end

```

```

if mod(j,2)==1
    y(76)=P1;
else
    y(76)=P0;
end
% -----

y(77:79) =P0; % assumed very high quality time
y(78)=P1; % assumed

%seconds of the days
% -----
secofday= x.sec+(60*x.mints)+(3600*x.hr);
seconds=zeros(17,1);
seconds(1:17)=sbs(secofday);
y(81:89)=seconds(1:9);
y(91:98)=seconds(10:17);

return

% =====

function y=bcd(d,n)
P0 = 1;
P1 = 2;
s=dec2bcd(d,n);
y=P0*ones(1,length(s)); % Set P0's
%y(find(s=='1'))=P1; % Set P1's
for si = 1:length(s)
    if (s(si) == '1')
        y(si) = P1;
    end
end
y=fliplr(y);
return

% =====

function y=bit(x)
P0 = 1;
P1 = 2;
if x, y=P1; else y=P0; end
return

% =====

function y=sbs(secofday)
%straight binary seconds of the day 17 digits

P0 = 1;
P1 = 2;
%coder.extrinsic('d2b');
coder.extrinsic('str2double');

s=blanks(17);

```

```

s=fliplr(d2b(secofday,17));

y=P0*ones(1,17);
for si = 1:17
    if (s(si) == '1')
        y(si) = P1;
    else
        y(si) = P0;
    end
end
y=fliplr(y);
return

% =====

function y=dec2bcd(d,n)
%DEC2BCD Convert decimal integer to a binary-coded-decimal (BCD) string.
% DEC2BCD(D) returns the BCD representation of D as a string.
% D must be a non-negative integer.
%
% DEC2BCD(D,N) produces a BCD representation with at least
% N decimal digits encoded.
%
% Example
%     dec2bcd(23) returns '00100011'
%     dec2bcd(23,3) returns '000000100011'
%
% See also d2b, BIN2DEC, DEC2HEX, DEC2BASE.

d = abs(d(:)); % Make sure d is a column vector.

digits = zeros(1,4);
if d<2,
    numdigits=1;
else
    numdigits=ceil(log10(d));
end

if nargin>1,
    if (numel(n)~=1) || (numdigits<0),
        error('N must be a positive scalar.');
```

```

if (n == 1)
    digits1=digits(4);
    y=zeros(1,4);
elseif (n == 2)
    digits1=digits(3:4);
    y=zeros(1,8);
elseif (n == 3)
    digits1=digits(2:4);
    y=zeros(1,12);
else
    digits1=digits;
    y=zeros(1,16);
end

for i=1:length(digits1),
    if (i == 1)
        y(1:4)=d2b(digits1(i),4);
    elseif (i == 2)
        y(5:8)=d2b(digits1(i),4);
    elseif (i == 3)
        y(9:12)=d2b(digits1(i),4);
    else
        y(13:16)=d2b(digits1(i),4);
    end
end

function s=d2b(d,n)
%   d2b(D,N) produces a binary representation with at least N bits.
%   Example d2b(23) returns '10111'
l=zeros(1,n);
s1=blanks(n);
for i=1:n
    l(i)=48;
    s1(i)=char(l(i));
end
l1=zeros(1,n);
i=0;
while d>=1
    i=i+1;
    p=rem(d,2);
    if p==0
        l1(i)=48;
        s1(i)=char(l1(i));
    else
        l1(i)=49;
        s1(i)=char(l1(i));
    end
    d=floor(d/2);
end
s=s1;
return

```

D Publications

- Singh, Ravi Shankar; Hooshyar, Hossein and Vanfretti, Luigi; "Assessment of time synchronization requirements for Phasor Measurement Units" in *PowerTech, 2015 IEEE Eindhoven*, June 29 2015-July 2 2015, pp.1-6.
- Singh, Ravi Shankar; Hooshyar, Hossein and Vanfretti, Luigi; "Laboratory Test Set-up for the Assessment of PMU Time Synchronization Requirements" in *PowerTech, 2015 IEEE Eindhoven*, June 29 2015-July 2 2015, pp.1-5.